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Four-Channel, High-Dynamic-Range Downconverter

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Final Report

November 1991

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Naval Research Laboratory
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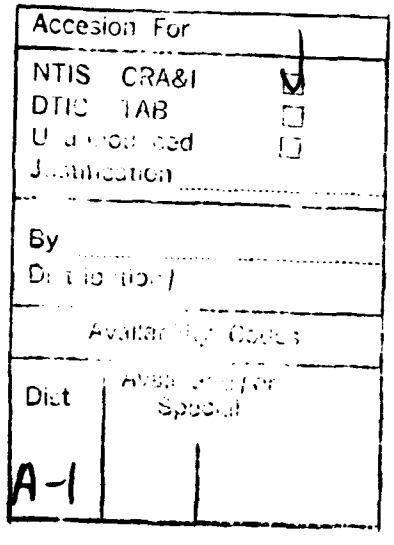

Final Report

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ABSTRACT

The David Sarnoff Research Center has developed, under a 24-month Naval Research Laboratory sponsored program, a four-channel, high-dynamic-range down-converter (HDRD) that will advance the state of the art in electronic warfare receivers by achieving a two-tone, spur-free dynamic range of 65 dB in a 50-MHz bandwidth. A spot check of the linear dynamic range measured 92 dB from the noise floor to the 1 dB compression point. There are several design features that lead to these excellent results. They include: (1) the use of wideband, low-noise, high intercept point MMIC amplifier chips for all of the amplifiers in the downconverter; (2) low-loss MMIC PIN-diode switches; (3) low-loss filters and diplexers; and (4) a high-dynamic-range mixer. The input frequency range of the HDRD is 6 to 18 GHz, and the output frequency (IF) is 3 to 5 GHz. It uses four local oscillator (LO) frequencies, 11, 13, 15 and 17 GHz, to downconvert the six, 2-GHz-wide subbands to the intermediate frequency. A switched filter bank, consisting of six 2-GHz-wide bandpass filters, provides the required frequency selection for the downconverter. Each branch of the filter bank includes an amplitude and phase trimming module to allow for the adjustment of the tracking among the four channels. The trimming module consists of T-pad attenuator chips and an adjustable length of 50-Ω transmission line. The attenuation is adjusted in 1-dB steps over a 1- to 6-dB range by selecting two attenuator chips, or one chip and a section of transmission line. The phase is adjusted by wire-bonding sections of transmission line together. This phase and amplitude trimming technique is also applied to the LO circuit. Although each mixer of the four-channel downconverter requires +20 dBm of LO power to achieve the high dynamic range, the total LO power input required is only 0 dBm due to the internal wideband LO amplifiers.

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Section I

INTRODUCTION

This is the final report on the four-channel, high-dynamic-range downconverter (HDRD) developed by the David Sarnoff Research Center for the Naval Research Laboratory (NRL), under contract number N00014-87-C-2495. The HDRD covers the 6- to 18-GHz band and achieves a two-tone, spur-free dynamic range of 65 dB and a remarkably high linear dynamic range (noise floor to 1-dB compression point) of 90 dB in a 50-MHz bandwidth. Although the instantaneous bandwidth of the downconverter itself is 2 GHz, it is assumed that most system applications would use the downconverter in front of a baseband processor that reduces the predetection bandwidth to something in the neighborhood of 50 MHz. Therefore, dynamic range measurements were made assuming a system predetection bandwidth of 50 MHz. Regardless of how dynamic range is calculated or measured, the subject downconverter represents a significant advancement in dynamic range capability.

Section II

DOWNCONVERTER DESIGN

The HDRD consists of four identical, 6- to 18-GHz downconverters that have an output frequency range (IF) of 3 to 5 GHz, and an instantaneous bandwidth of 2 GHz. The four channels are assembled in one housing that includes the dc power supply distribution circuits and regulators, the rf-switch signal decoding circuit, and the local oscillator (LO) power distribution network. A simplified block diagram of the HDRD is shown in Fig. 1. A more detailed block diagram of a single channel is shown in Fig. 2.

Preselection in the downconverter consists of dividing the signal path into two less-than-octave-wide bands, 6 to 10 GHz and 10 to 18 GHz, to filter out any out-of-band signals that can cause in-band harmonics and second-order intermodulation products.

Following the input filters are the low-noise amplifiers (LNA) that, along with the switch and filter, establish the noise figure of the downconverter. All of the amplifiers in the HDRD are GaAs, MMIC chips that require no tuning.

The input frequency range is divided into six subbands by a switched filter bank containing six bandpass filters. These subband filters are eight-pole, evanescant mode units with a 1-dB bandwidth of 2.5 GHz. A 0.25-GHz overlap in bandwidth is provided to avoid any bandedge group delay problems within the center 2-GHz portion of the passband.

The rf switches use a silicon, MMIC chip consisting of series/shunt PIN diodes with < 2-dB insertion loss and an isolation > 30 dB over the 6- to 18-GHz band.

The PIN diode switch drivers are hermetically sealed, hybrid microcircuits.

Each branch of the switched filter bank includes an amplitude and phase trimming module for the adjustment of the tracking among the four channels.

An isolator following the filter bank output switch provides a good match for the mixer rf port and increases the rf port isolation by about 14 dB.

The mixer is a high-dynamic-range, triple-balanced (double-double diode) unit that requires +20 dBm of LO power.

Terminating the mixer IF port is a highpass/lowpass diplexer.

The IF amplifier is a balanced configuration of cascaded, low-noise, MMIC amplifier chips.

At the IF port is a filter that attenuates the LO frequencies by ≥ 30 dB and has an insertion loss of less than 0.8 dB.

The externally-supplied LO power is divided into four, equal-phase signals and fed to each channel's mixer. The LO distribution network includes several MMIC amplifier chips to amplify the 0-dBm signal to the 20-dBm level required by the high-dynamic-range mixers.

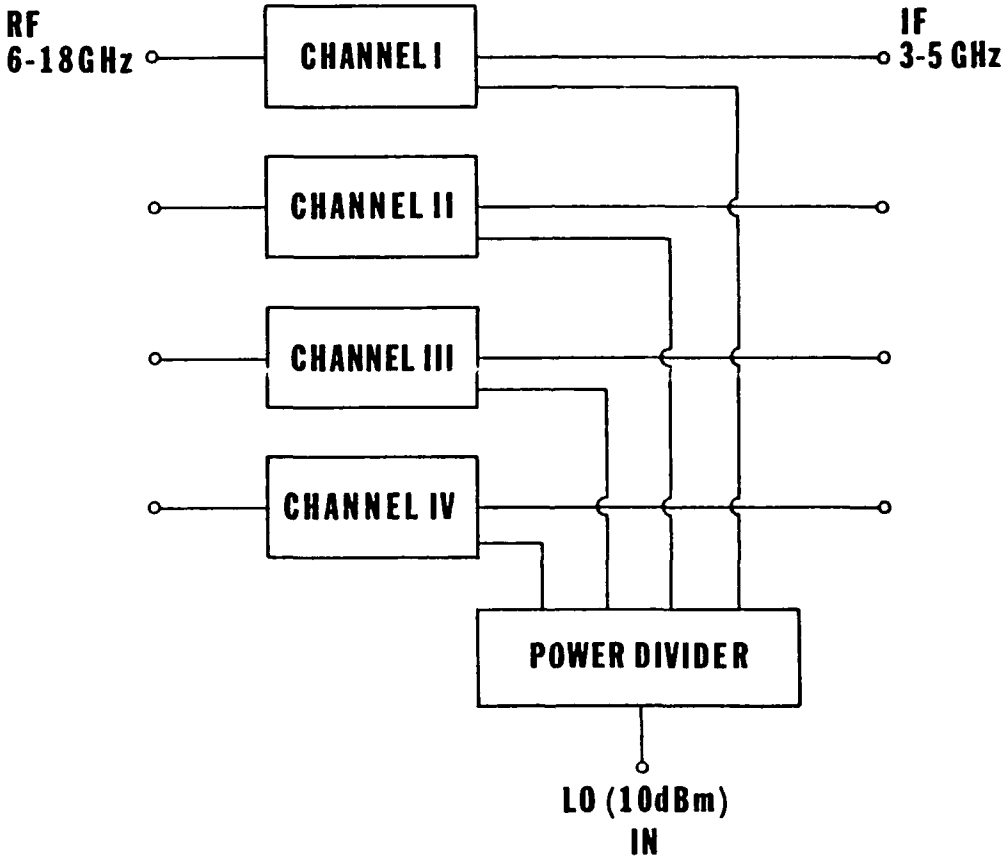


Figure 1. Block diagram of HDRD.

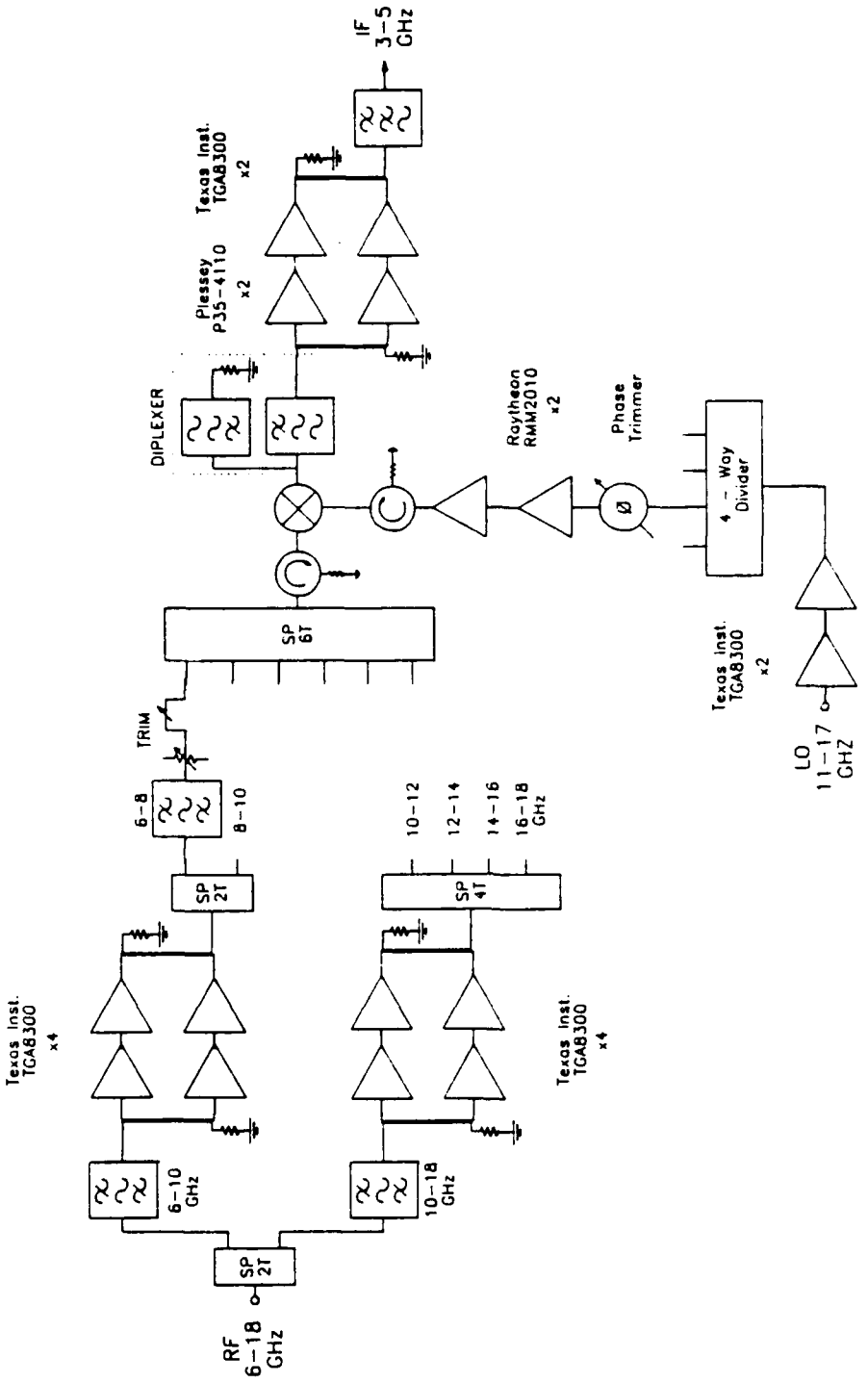


Figure 2. Single-channel block diagram of HDRD.

Section III

COMPONENTS

A. SPREAD SHEET ANALYSIS

An elecronic spread sheet was developed as a means of evaluating candidate components for the downconverter. Repeated calculation of the system performance, namely noise figure and spur-free dynamic range, was tedious and time consuming; and, if done manually, prone to error. The spread sheet, shown in Fig. 3, quickly calculated the effect of any component characteristic on the overall downconverter performance. This tool permitted the efficient exploration of many different components for the downconverter.

The spread sheet shows the name of each component along the top row with the component parameters in the column below its name.

The units used in the spread sheet are either dB or dBm, except for the temperature and bandwidth.

The column marked "System" (column C) shows the parameters for the complete downconverter channel as they are computed from the component data.

The data for the room-temperature noise figure of each component is entered in row 6 (NF @ 25 C). This value is converted to the noise figure at the ambient temperature entered in C3 (Ambient T). Row 4 (NF @ Amb.) shows the system- and component-noise figures at the ambient temperature.

The gain of the system (C5) is the sum of the gains (loss = negative gain) of each of the components. At this time the gain is not corrected for temperature deviation from the room-temperature value.

The bandwidth (C7), in this case 50 MHz, is the pre-detection bandwidth over which the noise floor is calculated.

The input intercept point (IIP) (row 9, IP3 in) is the output third-order intercept point (IP3 out) minus the component gain. The cascaded IIP (C9) of the system is calculated using Eq. (1)[1]:

$$IIP = 10*\log(1/(((1/IIP_1)+(G_1/IIP_2)+(G_1G_2/IIP_3)+...)), \quad (1)$$

where IIP_i is the IIP of the ith component and G_i is its gain.

The second-order IIP is not a concern in this system because any second-order products generated in the system fall outside the subband-filter bandwidth; therefore, any reference to IIP in this report will mean only the third-order IIP.

The Pin rows (11 and 12) show the signal level at the input to each component and the Pout rows (14 and 15), the output level. These are useful, for example, to assure that we do not overdrive the mixer, or that an amplifier can handle the input signal level without going into compression.

The system Pin min (C12) is a signal level that is equal to the noise floor (C18) at the input to the downconverter. Pin max (C11) is a level that is equal to the noise floor plus the calculated SFDR.

The system SFDR (C17) is computed using Eq. (2)[2]:

$$SFDR = 2/3[IIP - (- 114 + BW + NF)], \quad (2)$$

where IIP is the system input third-order intercept point (C9), BW is the pre-detection bandwidth (C7), and NF, the system noise figure (C4) at the ambient temperature shown in C3. This calculation shows the SFDR under the worst-case conditions since (1) assumes in-phase addition of all of the intermodulation products and (2) uses the noise figure at the highest estimated temperature of the system.

B. FILTER BANK SWITCHING

1. Switches

The rf switches use a monolithic, silicon chip that consists of a series/shunt pair of diodes. This Alpha Industries (model no. SSE3792) chip had the lowest insertion loss and highest isolation of the several diodes that were evaluated. In a SPST configuration, the maximum insertion loss over the 6- to 18-GHz band is 1.4 dB and the corresponding minimum isolation is 22 dB. The measured switching speed of a SPDT switch is less than 15 ns. The switching speed was measured in the setup shown in Fig. 4. Figure 5 shows oscillographs of the response of a SPDT switch at two different repetition rates. The output-third-order intercept point is ≤ 33 dBm at 18 GHz and the group delay is ≤ 0.3 ns.

A typical set of data measured on a SPDT switch are shown in Figs. 6 through 10. The markers in the figures are at 6 and 18 GHz, respectively. The insertion loss is typically < 1.4 dB at 18 GHz with an associated isolation of > 22 dB and a VSWR of < 2:1.

The insertion loss of the SP4T switch is 1.8 dB, maximum, and the isolation a minimum of 34 dB. The six-throw switch isolation is > 28 dB.

In the 16- to 18-GHz range, ports 1 and 6 of the six-throw switch have 2-dB more insertion loss than ports 2 through 5, but < 2 dB at lower frequencies. The signal paths through these switches are arranged so that only the low-frequency signals pass through ports 1 and 6, while the lower-loss ports, 2 through 5, are used for the higher frequencies.

Figures 11 through 14 show the performance of a typical SP6T. Figures 15 through 17 are photographs of the two-, four-, and six-throw switches, respectively.

The SPDT assembly measures 0.450 x 0.354 x 0.150 in. while the 4T and 6T units are 0.628 x 0.628 x 0.150 in.

2. Switch Drivers

The switch drivers used in the HDRD are constant-current devices from General Microcircuits Corporation (L230, L425 and L625). The drivers supply 25 mA to each diode of the pair. Figure 18 shows the switch drivers mounted on the regulator printed circuit board. The height of the driver flatpacks is adjusted to assure that they make contact with the bottom of the downconverter chassis for good heat sinking.

3. Switch Encoding

The switch control circuit is arranged to control all sixteen (16) rf switches through a single connector on the housing of the HDRD. The switches can be controlled from a computer or from the supplied control box.

C. LOW-NOISE AMPLIFIERS

All of the amplifiers in the HDRD are wideband, high-intercept-point, GaAs, MMIC amplifier chips. The LO amplifier chips are medium-power units, while the rf and IF amplifiers are low-noise parts.

Both the rf and the IF LNAs consist of four MMIC chips arranged between Lange couplers. Figure 19 is a photograph of the 6- to 10-GHz LNA, Fig. 20 the 10- to 18-GHz LNA, and Fig. 21 the IFA (3 to 5 GHz). In all cases, the input amplifiers are biased for low noise figure and the outputs for high intercept point. Paralleling the cascaded amplifiers in a balanced configuration with hybrid

couplers serves two purposes: primarily, a 3-dB improvement in the third-order intercept point over that of a single amplifier; and, secondarily, the couplers reduce the effect of the amplifier's VSWR on the external circuits. Parallel operation does not appreciably increase the noise figure over that of an individual device due to the incoherency of the noise.

The amplifier chip used in the rf LNAs (Texas Instrument, TGA8300) has a typical noise figure of 6.8 dB with 6.5 dB gain over the 6- to 18-GHz range. The output IP3 is, typically, +30 dBm.

Combining four of these chips in a balanced cascade, as shown in the above referenced figures, results in the data shown in Figs. 22 and 23.

The IFA input amplifier chip (Plessey, P35-4110-0) has a noise figure of 4.6 dB with 7.5-dB gain and an OIP3 of +30 dBm. A cascade of one Plessey chip and one TI chip in a balanced configuration typically provide the data shown in Fig. 24.

D. FILTERS

The subband filters are eight-pole, evanescent mode units, purchased from RS Microwave Company, Inc., that have a 1-dB bandwidth of 2.5 GHz and a 60-dB bandwidth of 7.5 GHz. The 60-dB stopbands extend down to dc and up to at least 18 GHz. The passband ripple is < 0.2 dB and the differential group delay is < 0.2 ns in any 500-MHz segment of the center 2 GHz of the passband.

While the desired passband is 2 GHz, this bandwidth was expanded by 500 MHz to ensure that the group-delay distortion that is caused by the bandedges will not occur within that passband.

E. PHASE AND AMPLITUDE TRIMMERS

Each branch of the switched filter bank includes an amplitude and phase trimming module to allow for the adjustment of the tracking among the four channels. The trimming module consists of a straight section of transmission line, an adjustable length of 50-Ω transmissiom line and, if required, one or two T-pad attenuator chips.

Figure 25 is a photograph of the phase and amplitude trimmer modules as installed in one of the downconverter channels.

1. Phase Trimmers

The phase trimmers are segments of microstrip transmission line that are bonded together with gold ribbon to adjust the relative insertion phase of each channel.

2. Amplitude Trimmers

The amplitude trimmer section provides space for the placement of one or two wideband, 50-Ω, attenuator chips from an assortment of 1-, 2-, or 3-dB units. The attenuation is adjusted in 1-dB steps over a 1- to 6-dB range by selecting two attenuator chips, or one chip and a section of transmission line.

F. MIXER

The mixer (Watkins-Johnson, MY88HC) is a high-dynamic-range, triple-balanced (double-double diode) unit that requires +20 dBm of LO power. It has an input-intercept point of about +26 dBm and a conversion loss of 7 dB over the 6- to 18-GHz frequency range. The mixer comes with removable SMA connectors, and when they and a spacer block are removed, the mixer becomes a surface-mountable part. The measured performance of the mixers purchased for the downconverter is shown in Tables 1 and 2.

G. ISOLATORS

There are two isolators in each downconverter channel. One (Sierra Microwave Technology, ADI6018A) is at the mixer rf-input port to provide a good source impedance for the mixer. This isolator reduces the LO leakage and any spurious mixer products at the mixer rf port by 14 dB. A second isolator (Mica Micrawave, SMF635-F1104) at the mixer LO port improves the match between the mixer and the LO amplifier, since the mixer has an LO-port VSWR that approaches 2.5:1 in the vacinity of the 13-GHz LO frequency.

H. LOCAL OSCILLATOR NETWORK

The HDRD has a single LO input port that requires a signal level of only 0 dBm to drive the mixers in all four channels.

The LO-signal amplification and distribution network includes low-noise and medium-power, MMIC amplifiers that amplify the externally supplied LO

TABLE 1

MIXER EVALUATION WJ MY88 HC
IP_3 VS RF FREQUENCY AND CONVERSION LOSS VS RF FREQUENCY

	LO DRIVE	INPUT IP_3 (dBm) IF = 4 GHz RF INPUT FREQUENCY						LO DRIVE	CONVERSION LOSS (dB) IF = 4 GHz RF INPUT FREQUENCY - GHz					
	dBM	7 GHz	9 GHz	11 GHz	13 GHz	15 GHz	17 GHz	dBm	7	9	11	13	15	17
Mixer #2	+19	+24.35	+24.10	+23.25	+25.50	+32.60	+23.45	+19	5.80	7.40	7.40	8.20	7.50	4.40
	+20	+27.70	+24.25	+27.75	+24.90	>+35	+23.75	+20	5.60	6.70	6.40	8.20	Did Not Measure	4.50
	+21	+27.10	+24.40	+22.95	+27.80	>+35	+24.15	+21	7.10	6.50	6.00	8.20	"	4.50
	+22	+27.15	+24.70	+21.55	+27.55	>+35	+23.40	+22	5.20	6.40	6.20	8.40	"	4.60
	+23	+27.55	+23.90	+20.85	+23.20	+33.30	+22.75	+23	5.30	6.40	6.70	8.50	6.50	4.80
Mixer #3	+19	+23.65	+24.30	+26.85	+19.20	+32.20	+25.50	+19	5.60	6.60	5.90	7.50	7.30	5.10
	+20	+24.45	+25.00	+25.10	+18.70	>+35	+26.70	+20	5.50	6.40	5.80	8.10	Did Not Measure	4.90
	+21	+25.85	+25.20	+24.10	+21.90	>+35	+26.05	+21	5.50	6.40	5.80	9.20	"	5.30
	+22	+26.60	+25.65	+22.25	+27.90	>+35	+24.95	+22	5.50	6.40	6.20	9.30	"	5.30
	+23	+26.80	+25.10	+16.55	+29.75		+23.60	+23	6.30	6.40	7.50	9.80	"	5.60
Mixer #4	+19	+23.65	+24.80	+26.65	+21.90	>+35	+25.25	+19	5.80	6.70	5.90	7.70		5.00
	+20	+25.30	+25.00	+23.45	+21.55	>+35	+25.70	+20	5.70	6.40	5.90	8.20	Did Not Measure	5.20
	+21	+25.95	+25.10	+21.85	+27.05	>+35	+25.70	+21	5.60	6.50	6.20	8.70	"	5.20
	+22	+25.50	+25.45	+19.70	+25.00	>+35	+24.50	+22	5.70	6.30	6.80	9.20	"	5.60
	+23	+26.30	+23.90	+19.75	+30.05		+23.10	+23	5.60	6.60	8.40	9.60	"	6.00

RF	LO
7	11
9	13
11	15
13	17
15	11
17	13

TABLE 2

	LO DRIVE	INPUT IP_3 (dBm) IF = 4 GHz RF INPUT FREQUENCY						LO DRIVE	CONVERSION LOSS (dB) IF = 4 GHz RF INPUT FREQUENCY - GHz					
	dBM	7 GHz	9 GHz	11 GHz	13 GHz	15 GHz	17 GHz	dBm	7	9	11	13	15	17
Mixer #5	+19	+24.90	+23.80	+24.50	+23.30	+32.40	+25.40	+19	5.90	6.60	5.90	8.10	7.50	4.90
	+20	+26.20	+24.45	+23.55	+22.50	+33.60	+25.70	+20	6.50	6.30	5.80	8.10	7.50	5.00
	+21	+27.40	+25.35	+21.75	+21.35	+35.10	+27.05	+21	5.70	6.10	6.00	8.30	7.10	5.10
	+22	+26.05	+26.15	+20.65	+26.40	+35.50	+25.10	+22	5.70	6.20	6.50	8.40	7.40	5.40
	+23	+26.55	+25.25	+18.50	+28.50	>+36	+24.60	+23	5.70	6.30	7.50	8.90	7.40	5.80

	LO DRIVE	INPUT IP_3 (dBm) IF = 4 GHz RF INPUT FREQUENCY						LO DRIVE	CONVERSION LOSS (dB) IF = 4 GHz RF INPUT FREQUENCY - GHz					
	dBM	7 GHz	9 GHz	11 GHz	13 GHz	15 GHz	17 GHz	dBm	7	9	11	13	15	17
Mixer #6	+19	+24.15	+23.60	+25.55	+24.55	>+35	+26.00	+19	6.00	6.50	6.20	8.50	6.60	5.20
	+20	+25.65	+24.25	+23.95	+22.35	+31.25	+26.65	+20	5.90	6.30	6.40	8.50	7.20	5.40
	+21	+27.00	+24.55	+21.90	+23.15	+32.85	+26.30	+21	5.70	6.10	6.60	8.70	6.80	5.30
	+22	+25.60	+24.60	+21.15	+29.70	+34.00	+25.25	+22	5.50	6.20	7.20	8.90	7.50	5.60
	+23	+28.45	+23.95	+18.10	+29.00	>+35	+23.35	+23	5.90	6.20	8.20	9.20	6.80	5.70

	LO DRIVE	INPUT IP_3 (dBm) IF = 4 GHz RF INPUT FREQUENCY						LO DRIVE	CONVERSION LOSS (dB) IF = 4 GHz RF INPUT FREQUENCY - GHz					
	dBM	7 GHz	9 GHz	11 GHz	13 GHz	15 GHz	17 GHz	dBm	7	9	11	13	15	17
Mixer #7	+19	+25.30	+23.15	+25.30	+22.95	+32.10	+26.00	+19	6.00	7.30	6.20	9.40	7.80	5.20
	+20	+25.70	+23.70	+23.10	+20.55	+33.40	+25.85	+20	5.90	7.00	6.40	9.60	7.60	5.10
	+21	+26.25	+24.55	+21.65	+25.70	+33.05	+26.00	+21	5.80	6.90	7.00	9.80	7.50	5.40
	+22	+27.00	+24.55	+21.20	+26.25	+33.30	+24.35	+22	5.80	6.80	7.80	10.00	7.30	5.80
	+23	+26.25	+24.60	+20.20	+31.55	+31.80	+23.05	+23	5.80	6.80	8.40	10.60	7.60	6.00

signal from 0 dBm to +20 dBm at the mixer LO port. A two-stage, medium-power amplifier (Raytheon, RMM2010), shown in Fig. 26 is included with each channel. A plot of one amplifier's noise figure and small-signal gain is shown in Fig. 27. The 1-dB compression point for these amplifiers is +20 to +21 dBm at each of the LO frequencies. A separate two-stage, low-noise pre-amplifier (Texas Instruments, TGA8300), followed by a one-stage medium-power amplifier, is provided to boost the signal before it is divided by a four-way divider (Vectronics Microwave, PD10180-4MR) for distribution to each channel.

The LO distribution network includes a coaxial phase trimmer (Midisco, MDC 1089-2) in each of the cables between the four-way power splitter and the individual channels to adjust all four cables to the same electrical length.

I. DIPLEXER

A diplexer is located between the mixer and the IF amplifier. The purpose of the diplexer is to absorb all mixer output frequencies above the IF band so they will not be reflected back to the mixer to possibly generate additional unwanted spurious products, which would happen if a lowpass filter were used alone.

The highpass section of the diplexer passes signals > 6.3 GHz and terminates them in a 50-Ω load, while the lowpass section passes signals ≤ 5.25 GHz.

The highpass filter is an interdigitated, suspended-substrate design, and the lowpass filter is a hybrid (microstrip and lumped-element) filter on 15-mil-thick alumina. The series inductive sections are in microstrip and the shunt capacitance is provided by chip capacitors.

A photograph of the diplexer is shown in Fig. 28. Figures 29 and 30 show the frequency response.

J. BANDSTOP FILTER

The IFA is followed by a bandstop filter at the downconverter output port. The purpose of this filter is to increase the rejection of the LO signal and any other spurious products > 5 GHz that might reach the IF output. This filter is a microstrip circuit on 15-mil-thick alumina. It consists of four open-circuited stubs on a high-impedance, series transmission line. A drawing of the filter is shown in Fig. 31. Figure 32 is a plot of the passband response where the insertion

loss in the 3- to 5-GHz band is < 0.75 dB. Figure 33 shows the stopband response with the four LO frequencies indicated by the markers. The LO rejection is ≥ 30 dB. The VSWR of the filter is shown in Fig. 34, where the passband match is 1.5:1. These data include the test fixture losses.

K. VOLTAGE REGULATORS

The downconverter operates from -3 and +10-V dc for the MMIC amplifiers and ±5 V for the switch control logic. The total dc input power is 98 W for the four-channel system. Figures 35 and 36 show each side of the voltage regulator/switch driver PC board.

L. HOUSING

All four channels are assembled in one housing that includes the dc bias voltage regulators for the amplifiers as well as the decoding logic for the TTL switch control voltages.

Figure 37 is a photograph of the HDRD housing with the top cover removed. It is a view of the rf input side showing the isolators that were installed to provide a good input match to each downconverter channel.

Figure 38 is a view of the IF output side of the housing showing the switch control box cable, the dc power input "D" connector, and the LO signal input connector.

An angular view of the bottom of the housing, with the cover removed, is shown in Fig. 39. Figure 40 is another view of the bottom of the housing where the 25-wire ribbon lead of the rf switch control circuit is most prominent. The narrower ribbon leads are for the dc supply voltages. This view also shows the four-way power splitter, the coaxial phase trimmers in the LO cables, and the LO pre-amplifiers.

A top view of one of the downconverter channels is displayed in of Fig. 41, and Fig. 42, the bottom view, showing the voltage regulator/switch driver PC board.

A single channel, with the top cover removed, is shown in Fig. 43.

The size of the HDRD is 14.5 x 19 x 2 in., not including the connectors.

M. SUBBAND SWITCH CONTROL BOX

A separate switch box controls the 16 rf switches of the downconverter with a single, six-position, subband-select knob. The switching system could also be controlled by a computer since the control input is negative TTL logic; that is, grounding the desired subband control line sets up all of the switches for the selected subband.

	MRL9r	C	E	F	G	H	I	J	K	L	M	O	Q	R	S	T	U	V	W	
2	FR CH DC	SYSTEM	ISO	SWITCH	BPF	LNA	SWITCH	BPF	TRIM	SWITCH	ISO	MIXER	DIPLEXR	IF AMP	IF AMP	LPF	TOTALS	UNITS	Parameter	2
3	Ambient T.	55.00		2-13-89														Deg C	Ambient T.	3
4	NF @ Amb	10.47	0.00	1.41	0.55	5.30	1.41	0.98	1.09	1.41	1.09	7.35	0.66	5.09	5.09	1.09	10.47	dB	NF @ Amb	4
5	Gain	9.10	0.00	-1.30	-0.50	13.00	-1.30	-0.90	-1.00	-1.30	-1.00	-7.00	-0.60	6.00	6.00	-1.00	9.10	dB	Gain	5
6	NF @ 25 C		0.00	1.30	0.50	5.00	1.30	0.90	1.00	1.30	1.00	7.00	0.60	4.80	4.80	1.00		dB	Noise Fig.	6
7	Bandwidth	50.00															50.00	MHz	Bandwidth	7
8	IP3 out	26.55	100.00	100.00	100.00	35.00	100.00	100.00	100.00	100.00	100.00	20.00	100.00	33.00	33.00	100.00	26.55	dBm	IP3 out	8
9	IP3 in	17.45	100.00	101.30	100.50	22.00	101.30	100.90	101.00	101.30	101.00	27.00	100.60	27.00	27.00	101.00	17.45	dBm	IP3 in	9
10																				
11	Pin max	-17.21	-17.21	-17.21	-18.51	-19.01	-6.01	-7.31	-8.21	-9.21	-10.51	-11.51	-18.51	-19.11	-13.11	-7.11	-17.21	dBm	Pin max	11
12	Pin min	-86.54	-86.54	-86.54	-87.84	-88.34	-75.34	-76.64	-77.54	-78.54	-79.84	-80.84	-87.84	-88.44	-82.44	-76.44	-86.54	dBm	Pin min	12
13																				
14	Pout max	-8.11	-17.21	-18.51	-19.01	-6.01	-7.31	-8.21	-9.21	-10.51	-11.51	-18.51	-19.11	-13.11	-7.11	-8.11	-8.11	dBm	Pout max	14
15	Pout min	-77.44	-86.54	-87.84	-88.34	-75.34	-76.64	-77.54	-78.54	-79.84	-80.84	-87.84	-88.44	-82.44	-76.44	-77.44	-77.44	dBm	Pout min	15
16																				
17	S.F.D.R.	69.32				76.01						78.01		79.47	79.47		69.32	dB	S.F.D.R.	17
18	Noise Flr	-86.54	-97.01	-95.71	-96.51	-92.01	-95.71	-96.11	-96.01	-95.71	-96.01	-90.01	-96.41	-92.21	-92.21	-96.91	-86.54	dBm	Noise Flr	18
19																				

Figure 3. System analysis spread sheet.

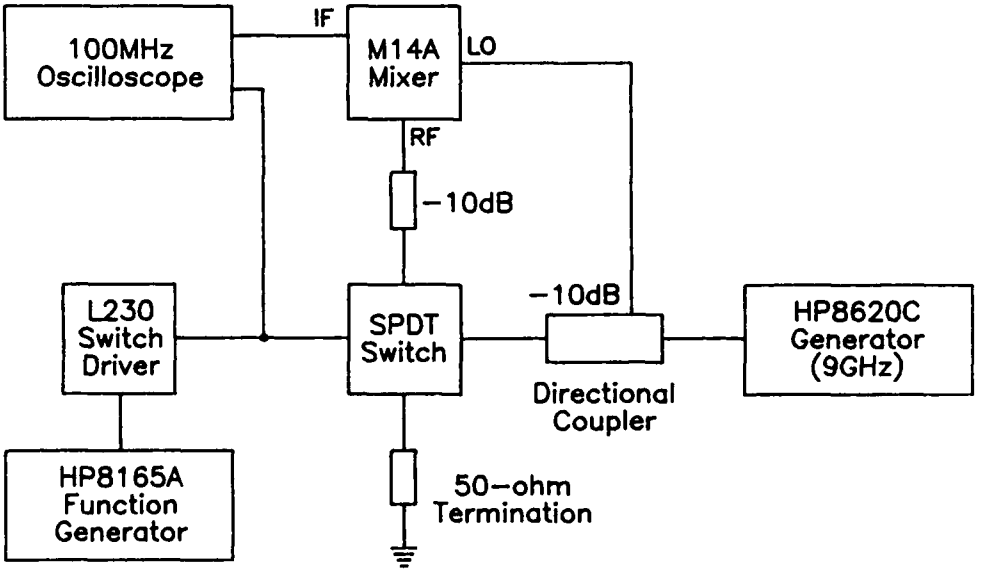


Figure 4. Test setup for measuring switching speed.

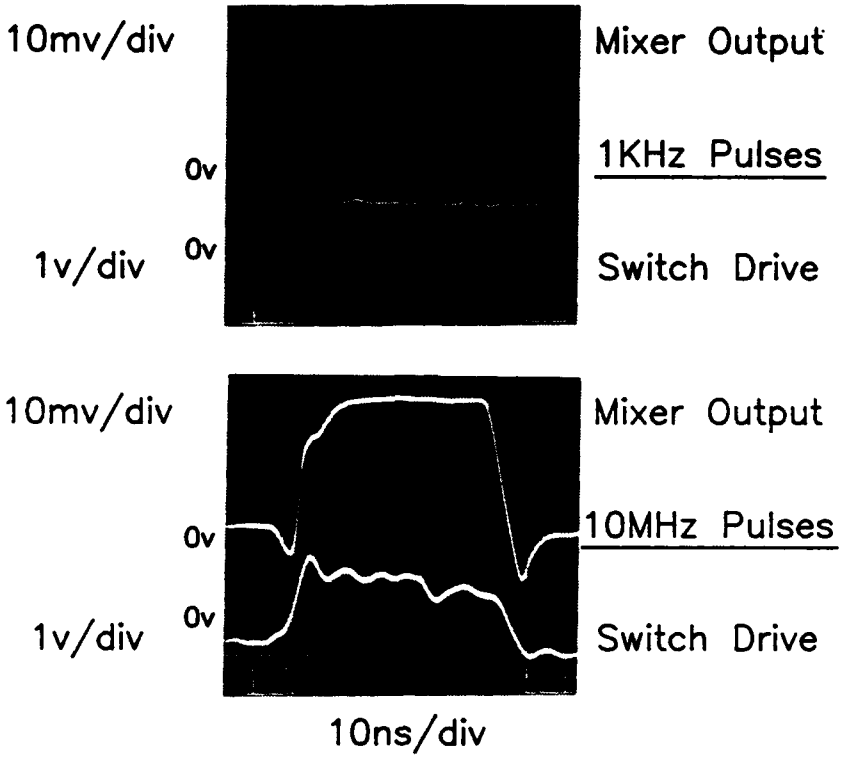


Figure 5. Switching speed of SPDT switch.

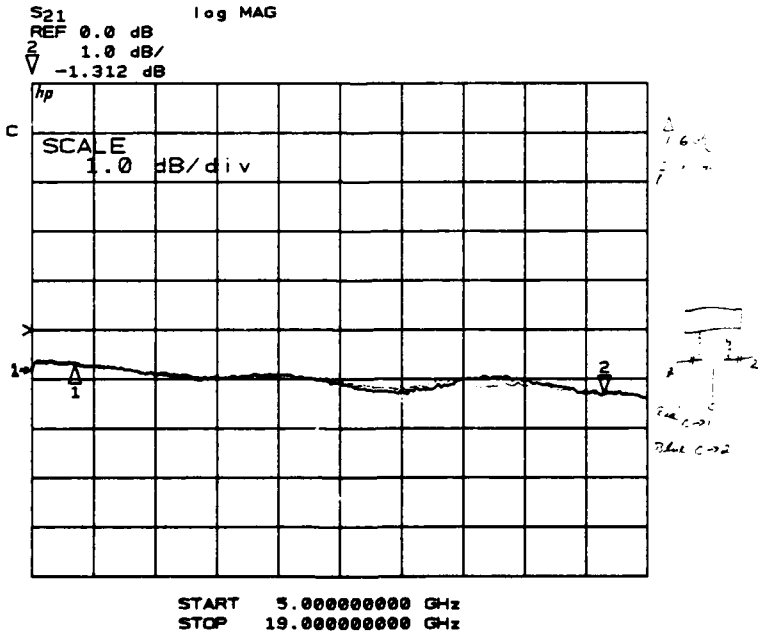


Figure 6. SPDT switch, insertion loss vs frequency.

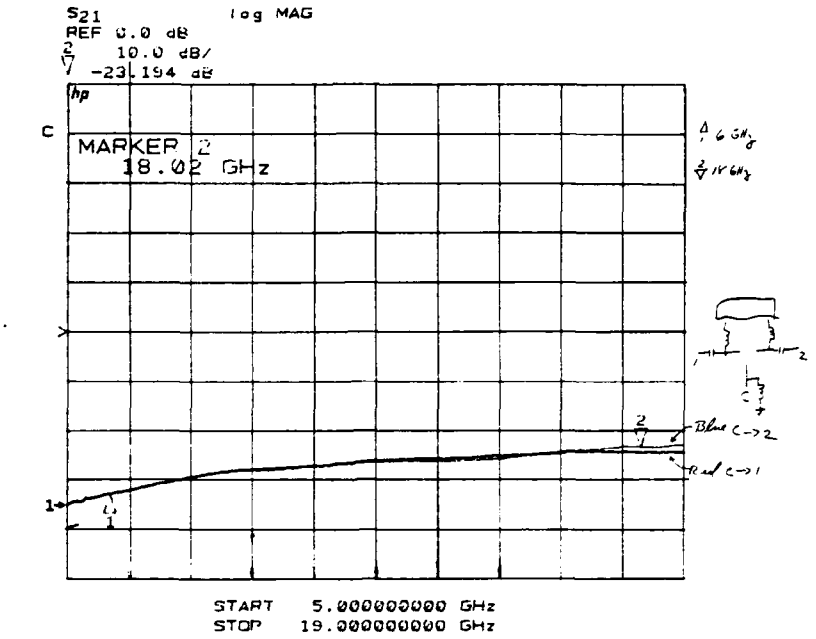


Figure 7. SPDT switch, isolation vs frequency.

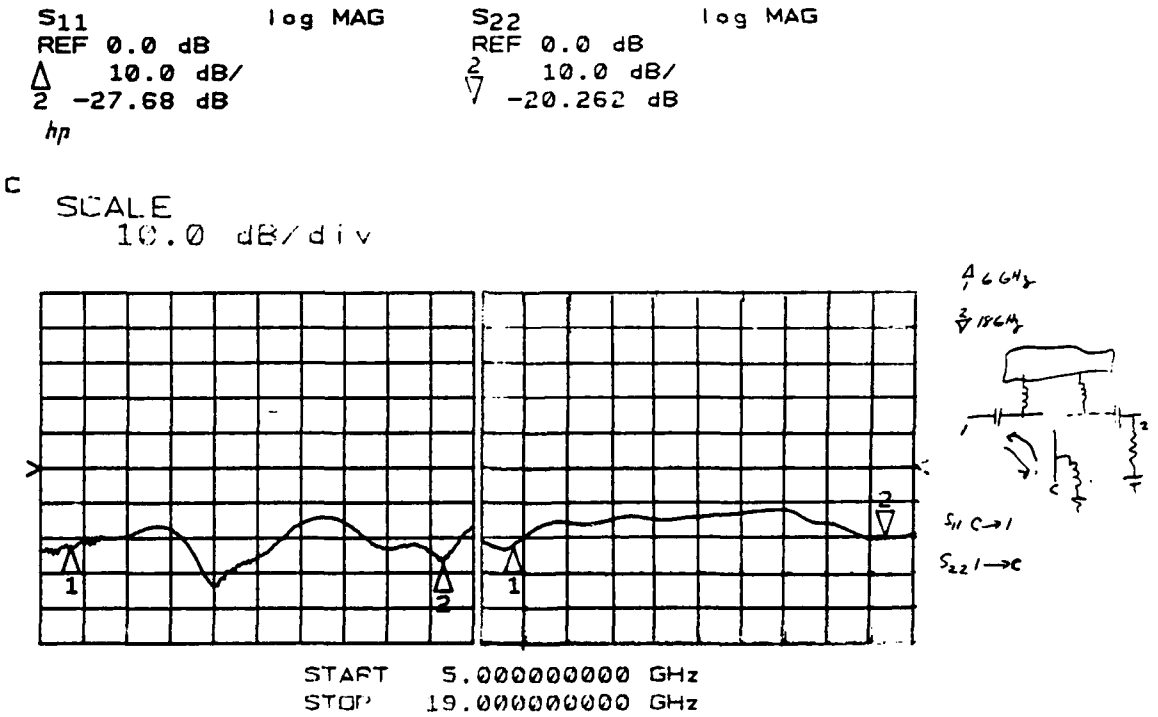


Figure 8. SPDT switch, return loss vs frequency, port 1.

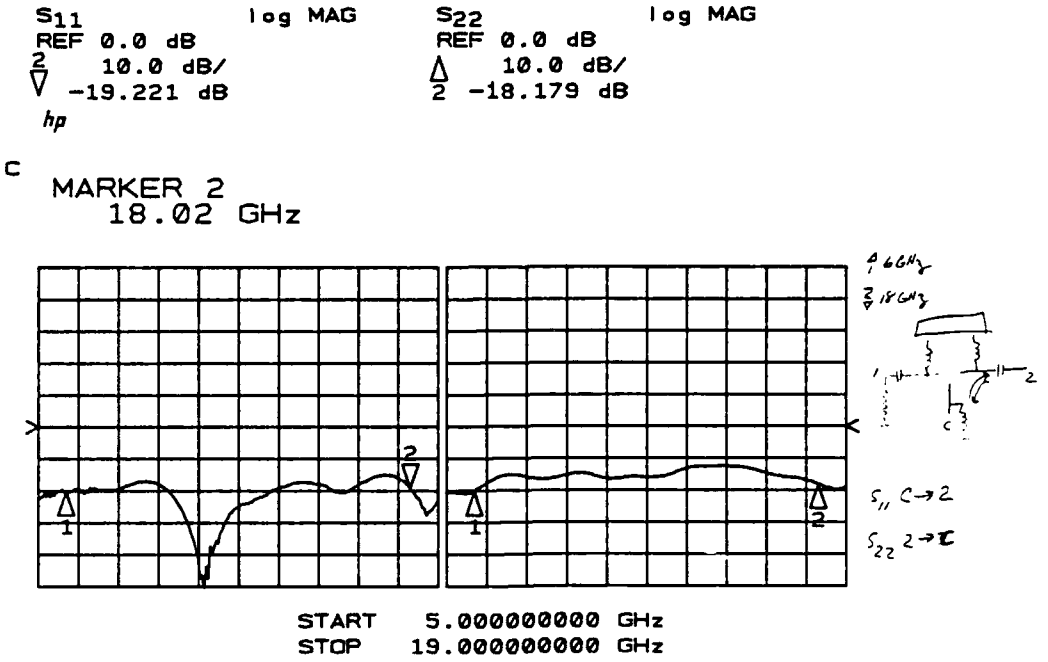


Figure 9. SPDT switch, return loss vs frequency, port 2.

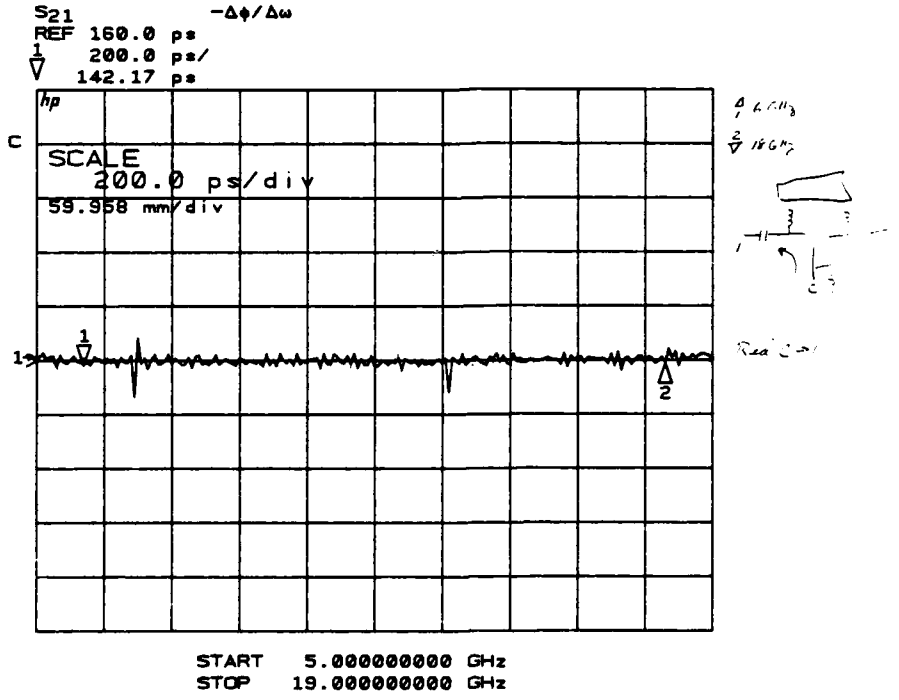


Figure 10. SPDT switch, group delay vs frequency.

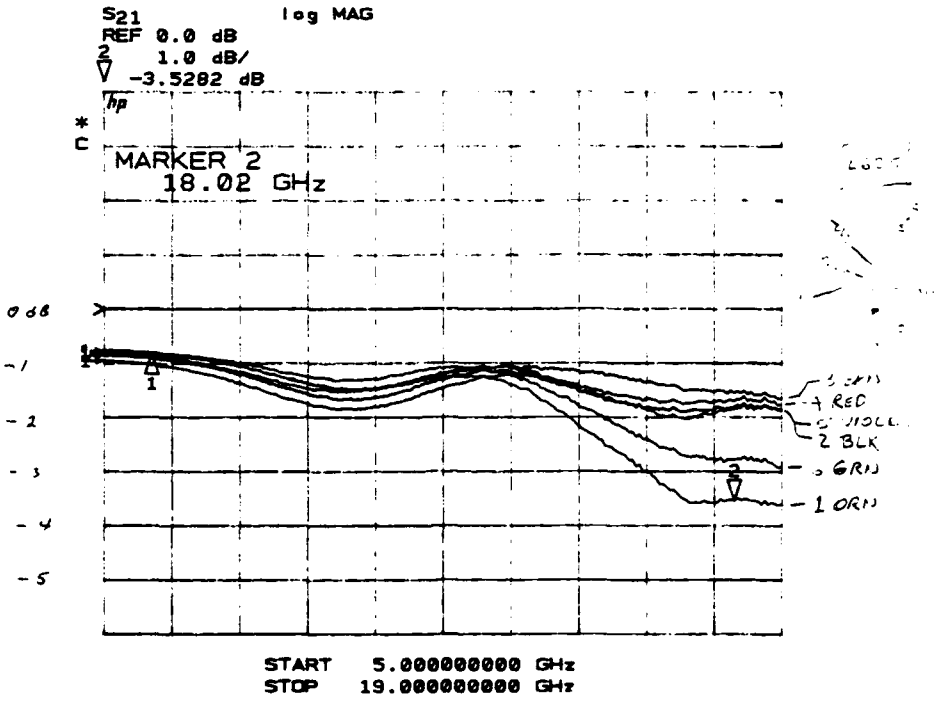


Figure 11. SP6T switch, insertion loss vs frequency.

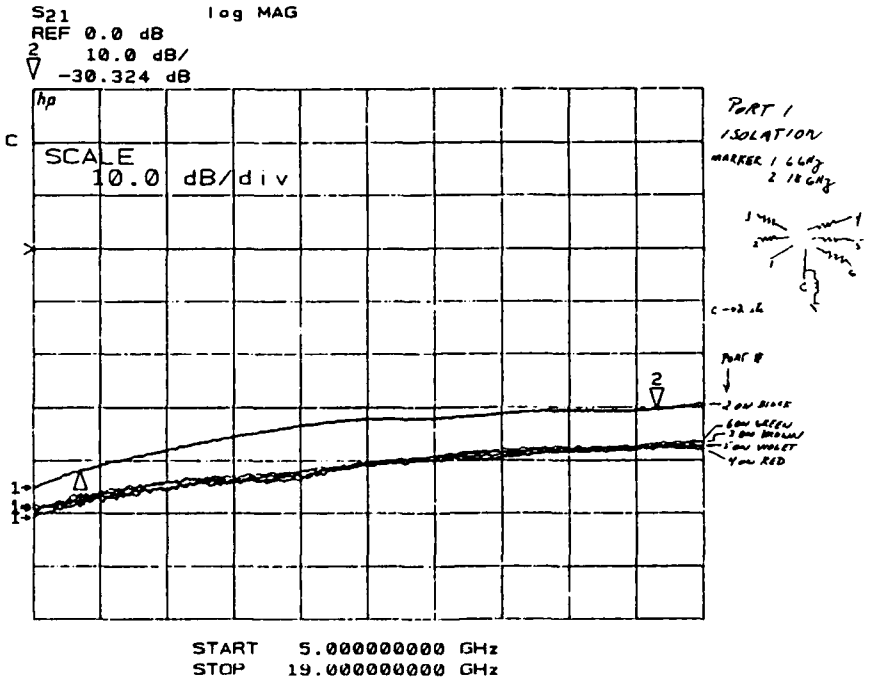


Figure 12. SP6T switch, isolation vs frequency.

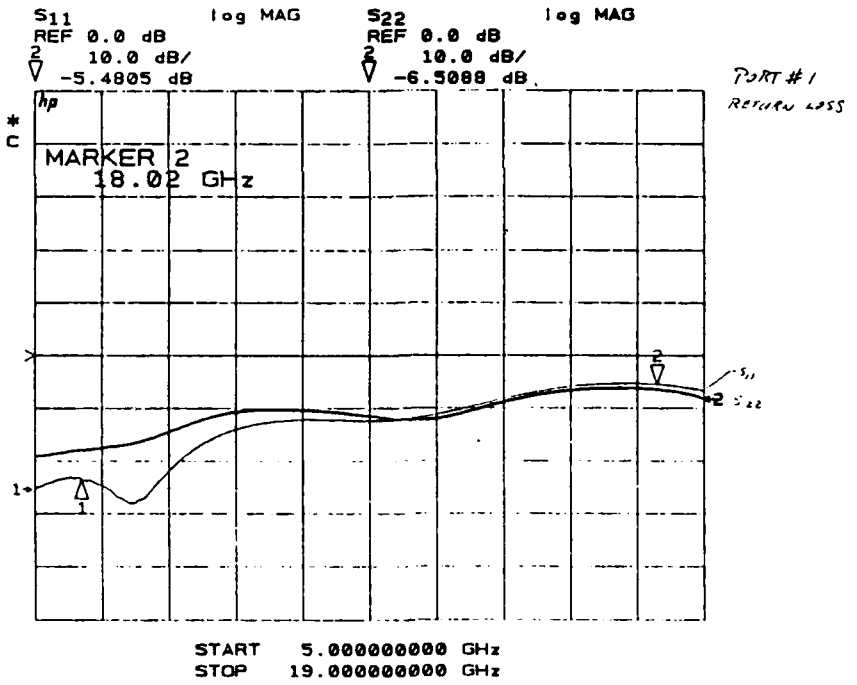


Figure 13. SP6T switch, return loss vs frequency.

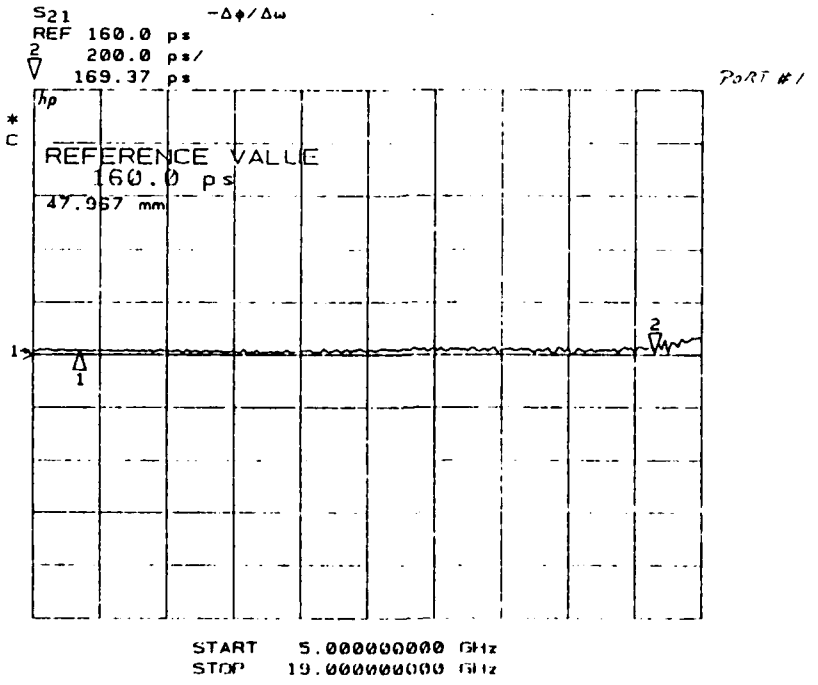


Figure 14. SP6T switch, group delay vs frequency.

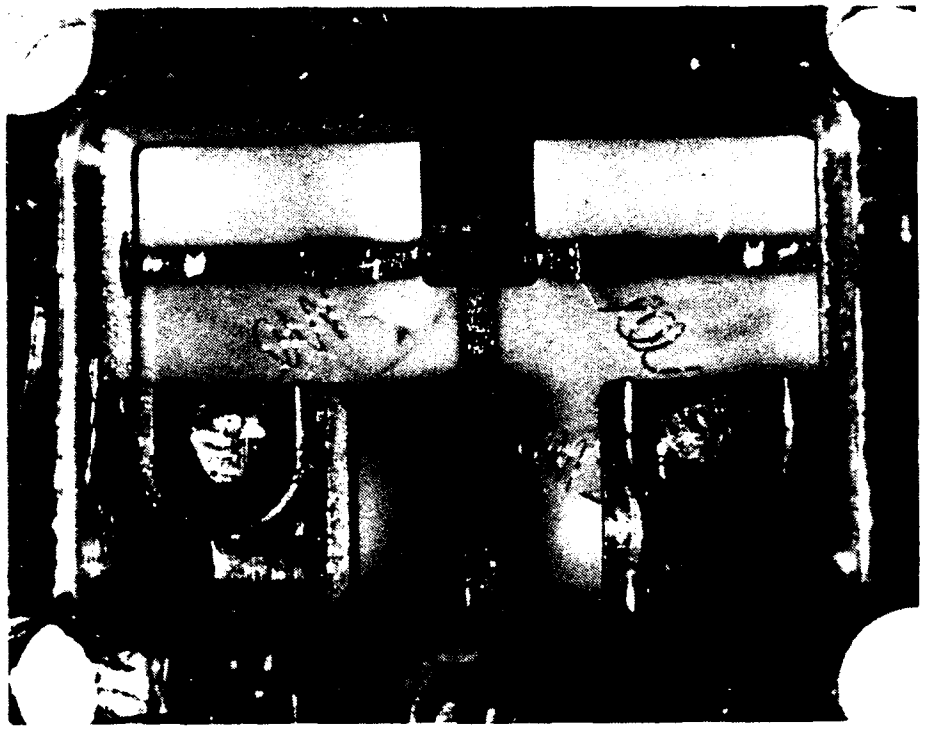


Figure 15. Photograph of SPDT switch.

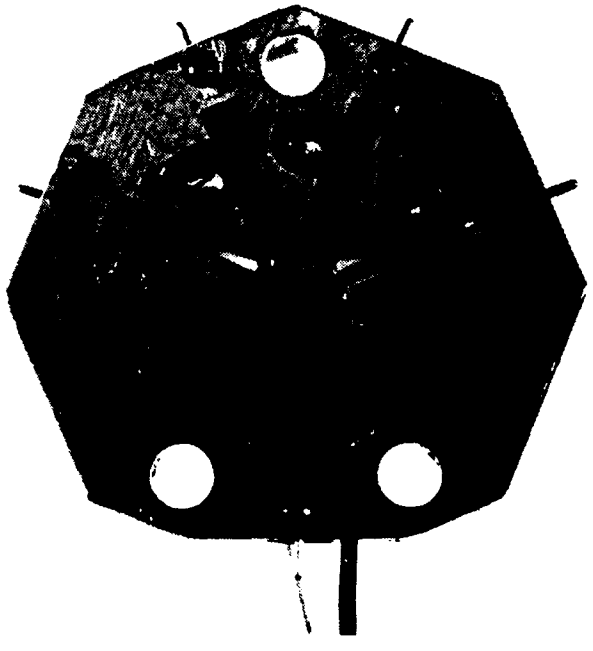


Figure 16. Photograph of SP4T switch.

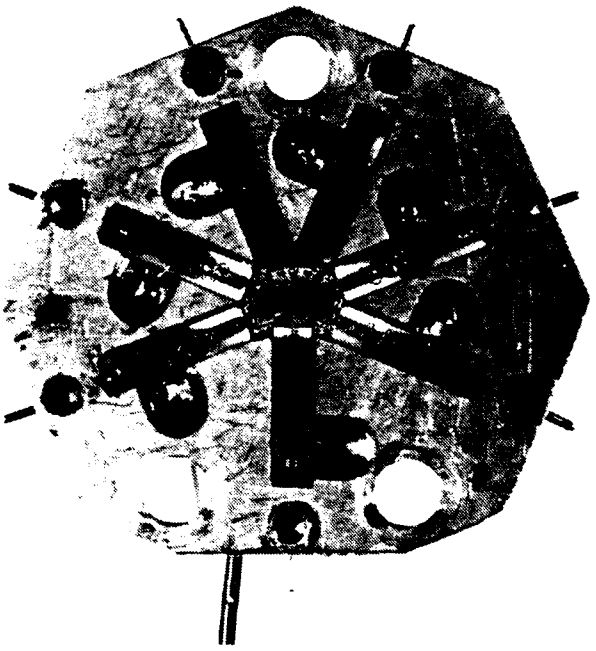


Figure 17. Photograph of SP6T switch.

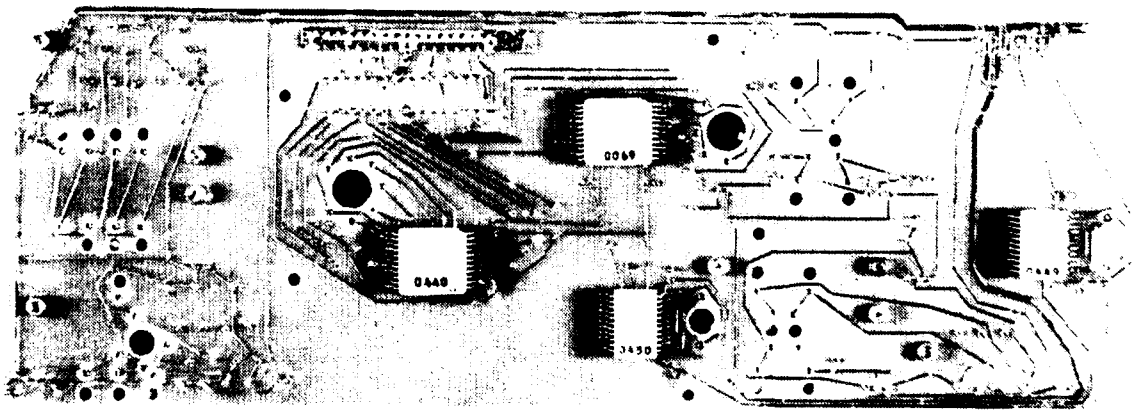


Figure 18. Voltage regulator/switch driver PC board, conductor side.

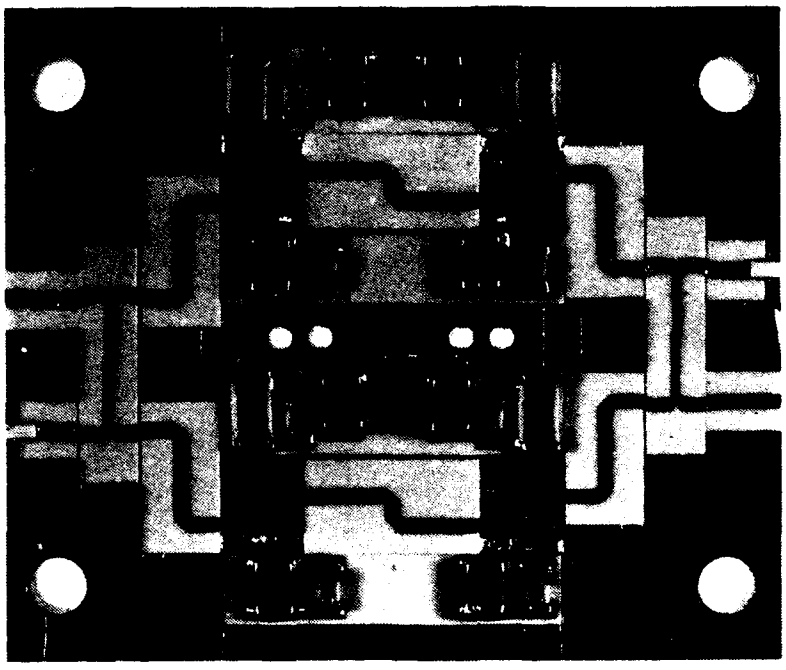


Figure 19. 6- to 10-GHz LNA.

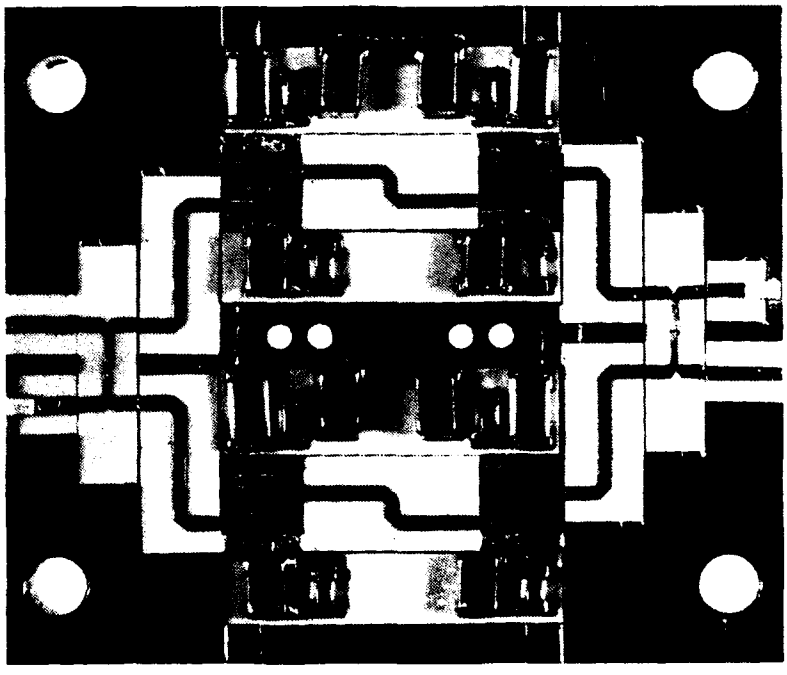


Figure 20. 10- to 18-GHz LNA.

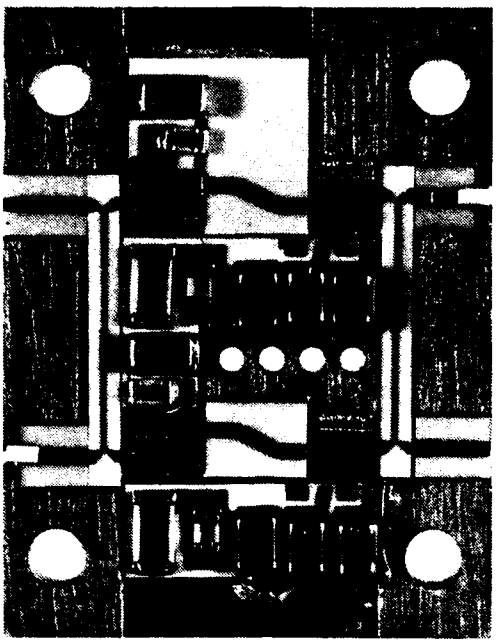


Figure 21. 3- to 5-GHz IF LNA.

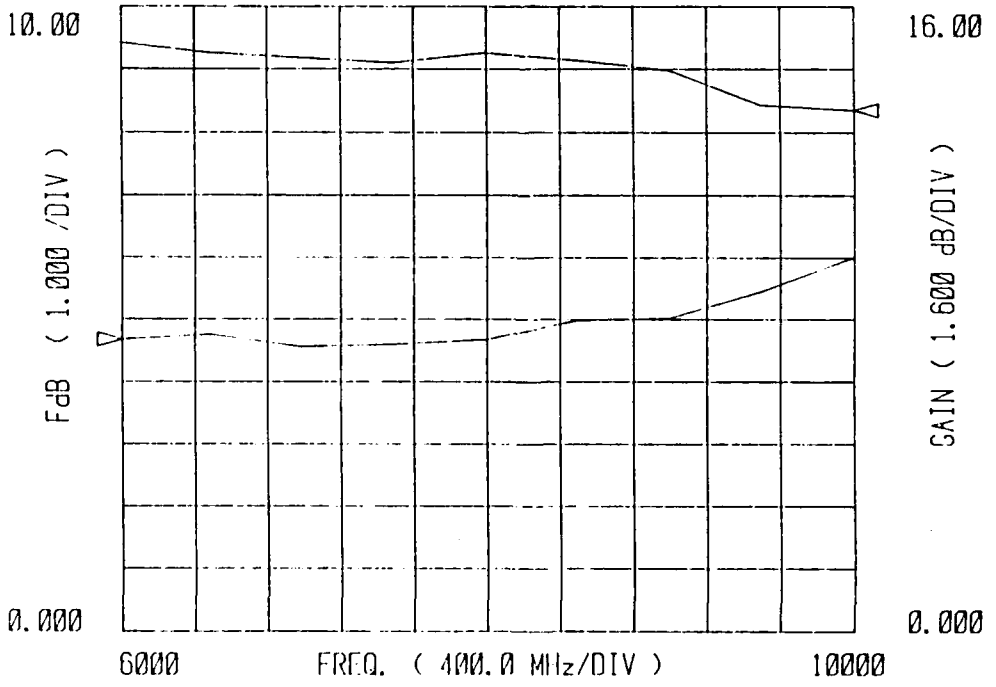


Figure 22. Noise figure and gain of 6- to 10-GHz LNA.

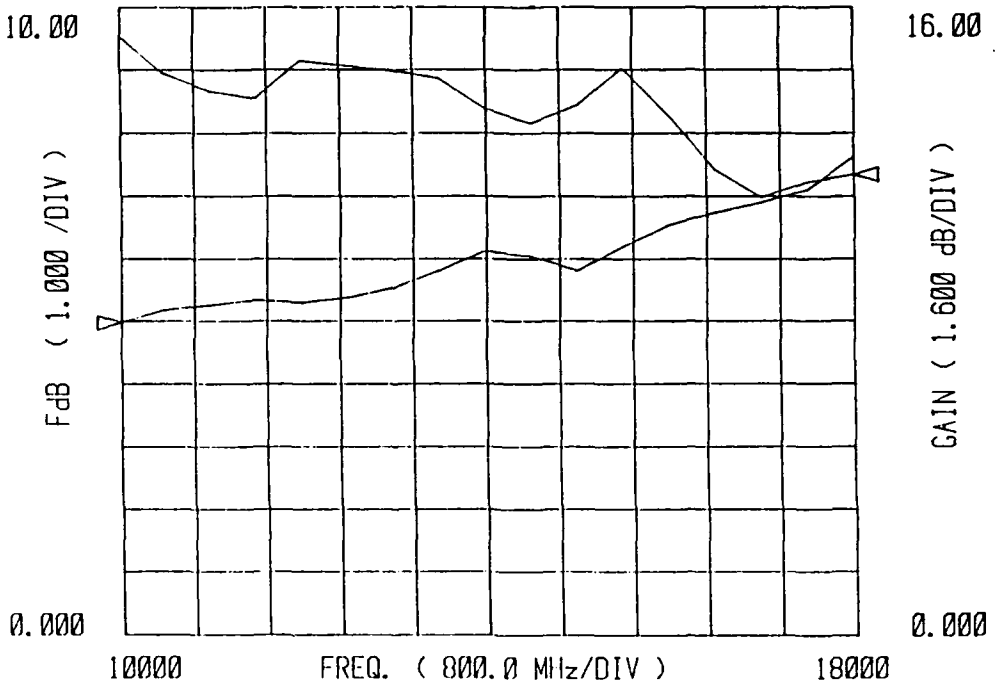


Figure 23. Noise figure and gain of 10- to 18-GHz LNA.

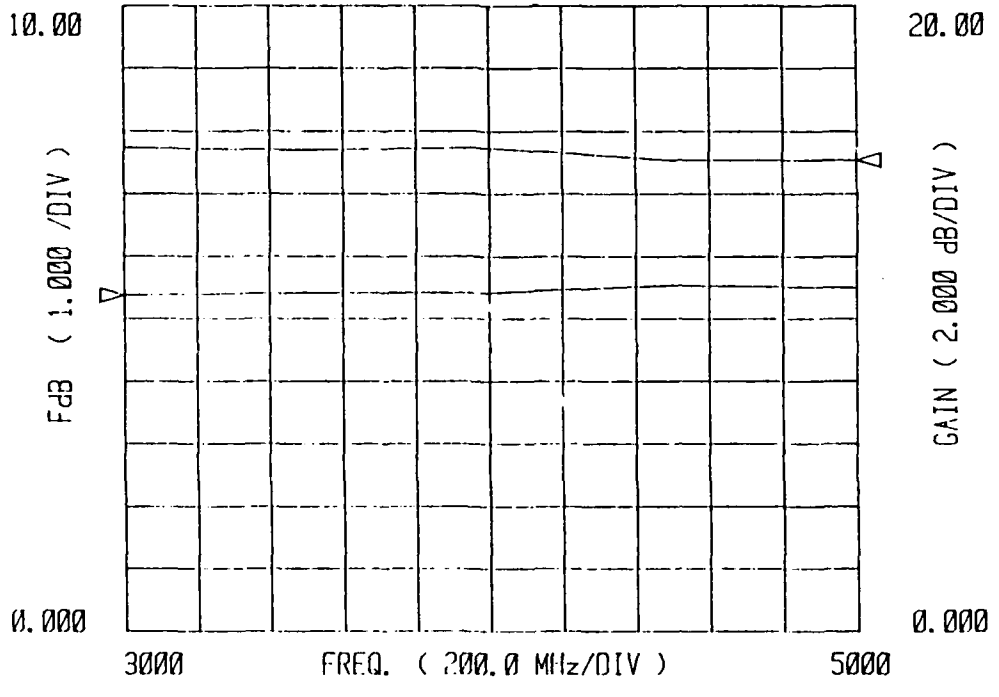


Figure 24. Noise figure and gain of 3- to 5-GHz IF LNA.

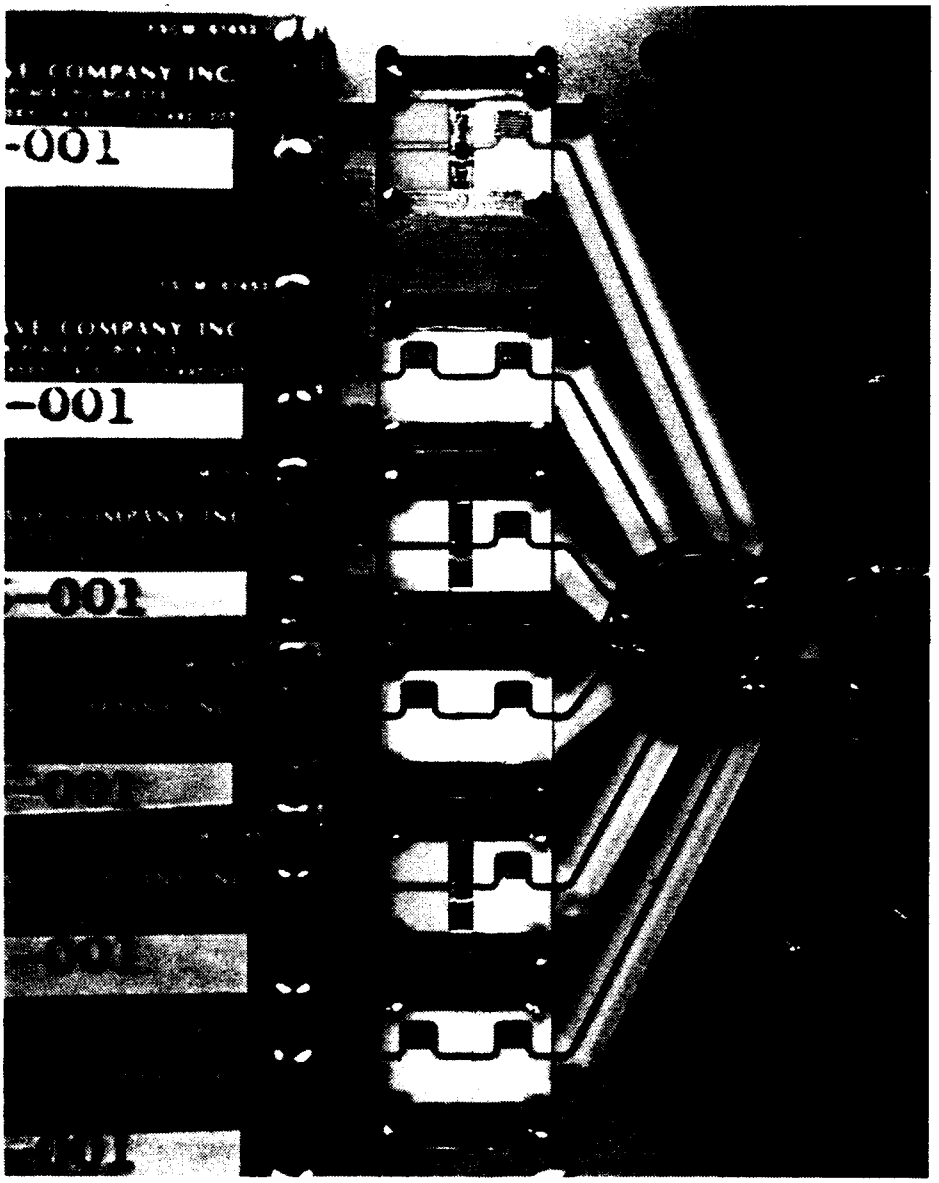


Figure 25. Phase and amplitude trimmer modules, installed in channel 1.

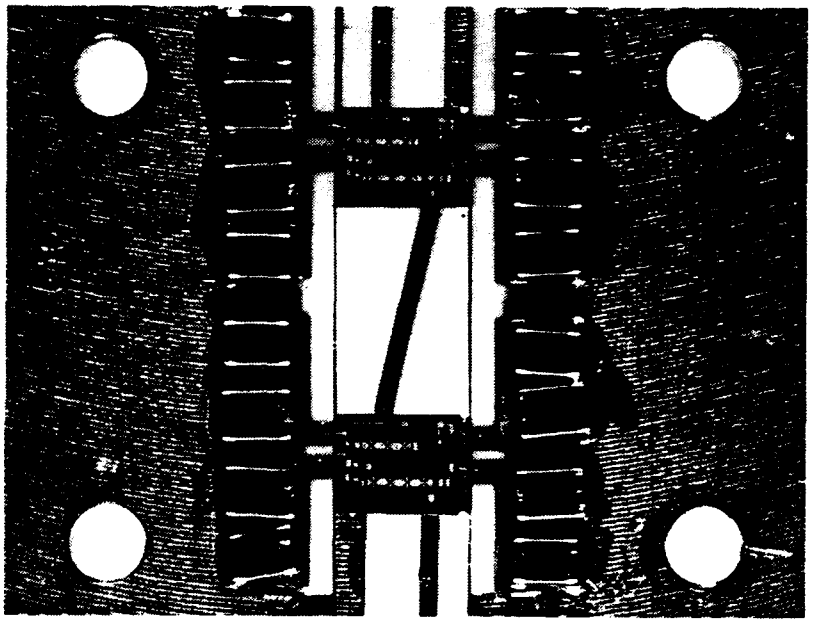


Figure 26. Local oscillator amplifier, 11 to 17 GHz.

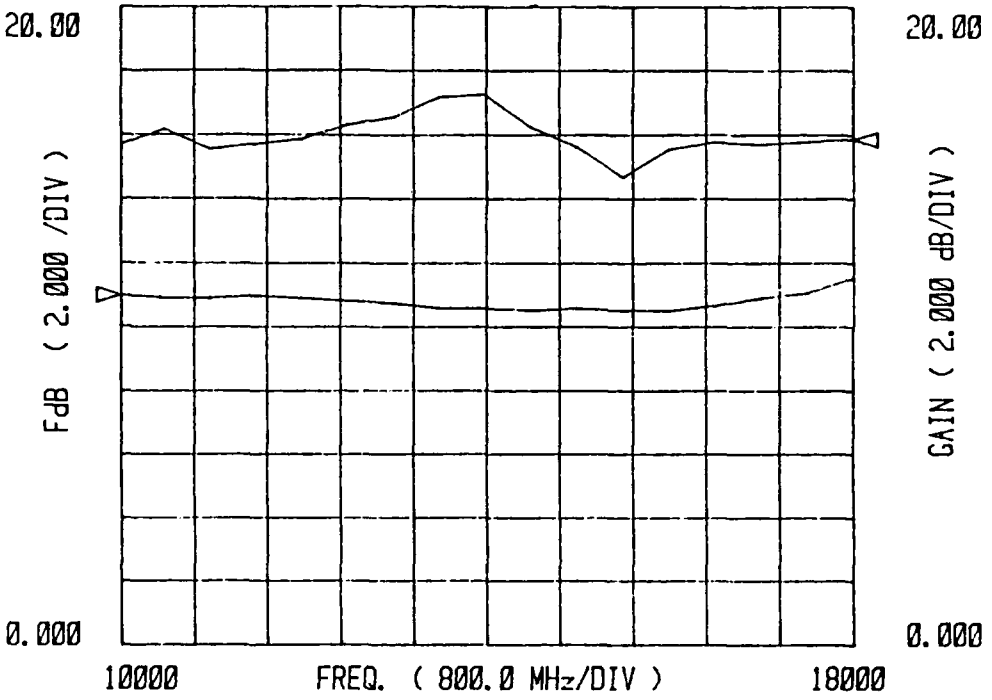


Figure 27. Noise figure and small signal gain of LO amplifier.

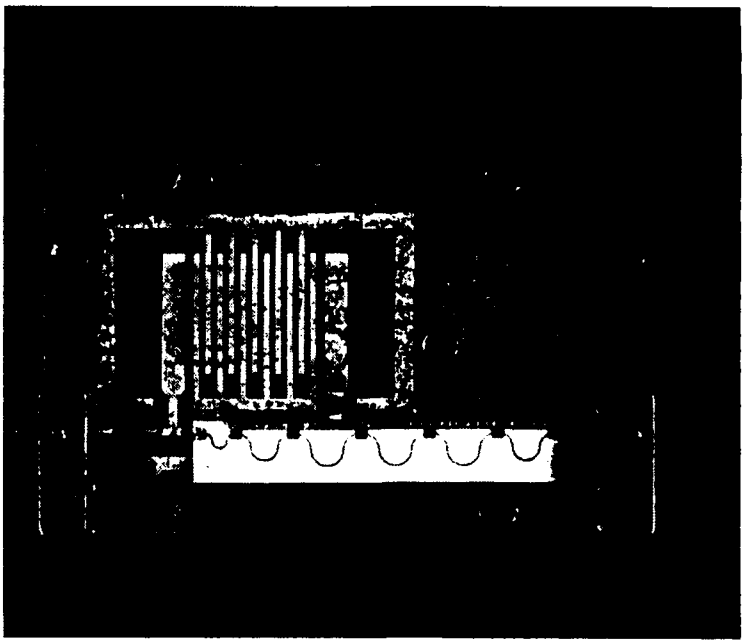


Figure 28. Photograph of diplexer.

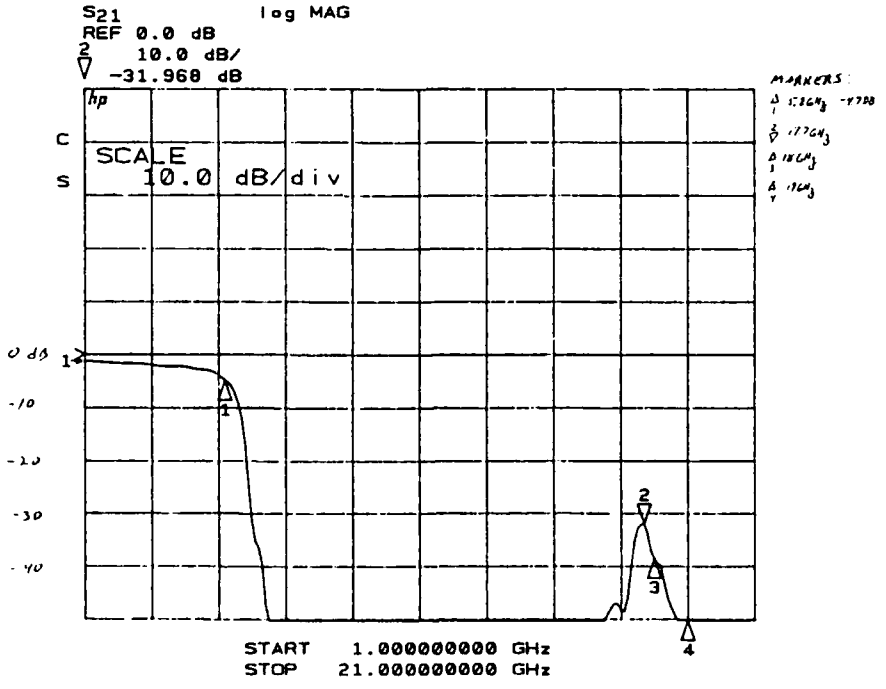


Figure 29. Diplexer, insertion loss vs frequency.

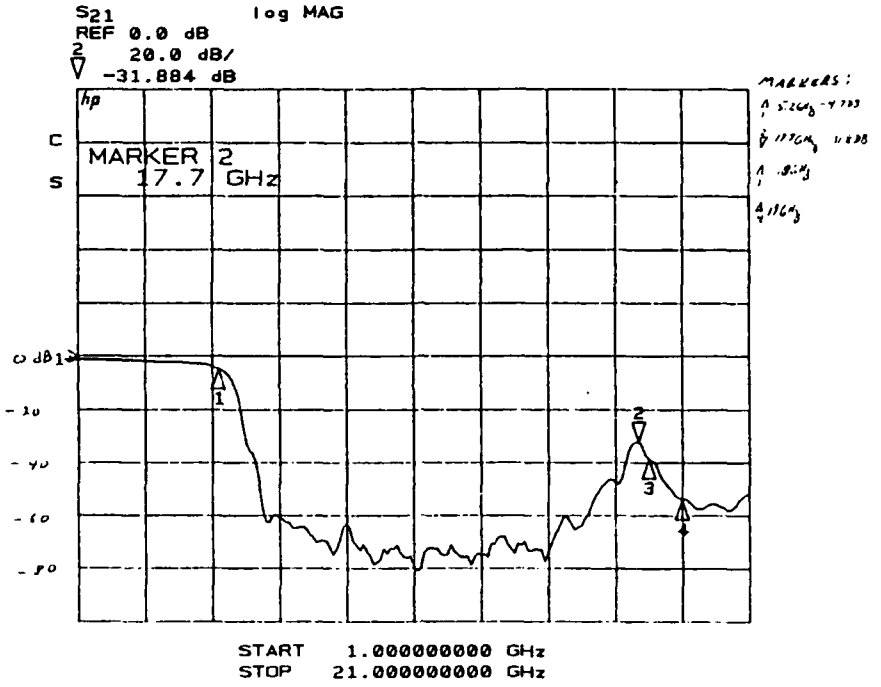


Figure 30. Diplexer, attenuation vs frequency.

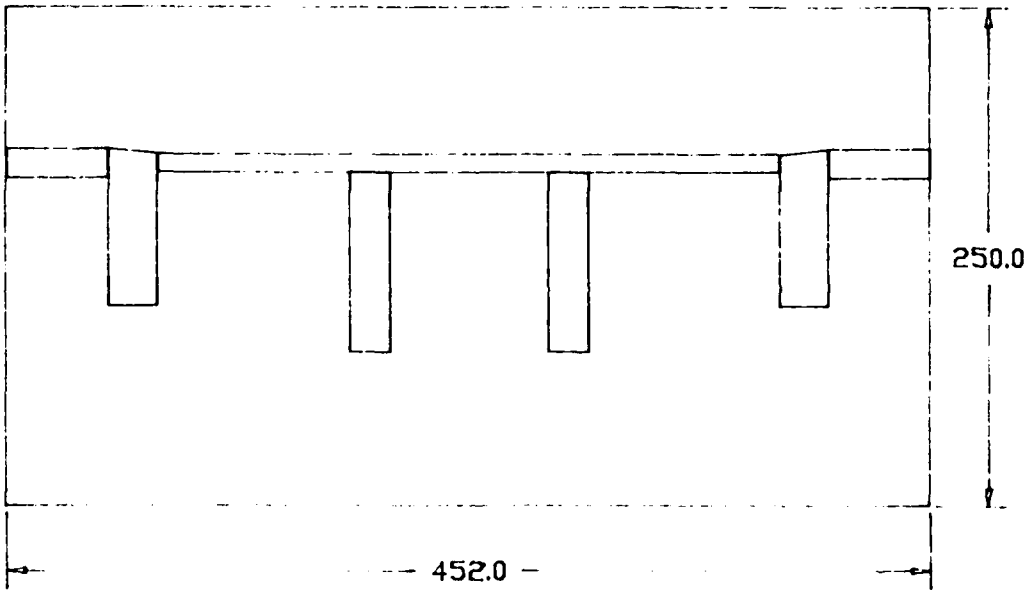


Figure 31. Bandstop filter.

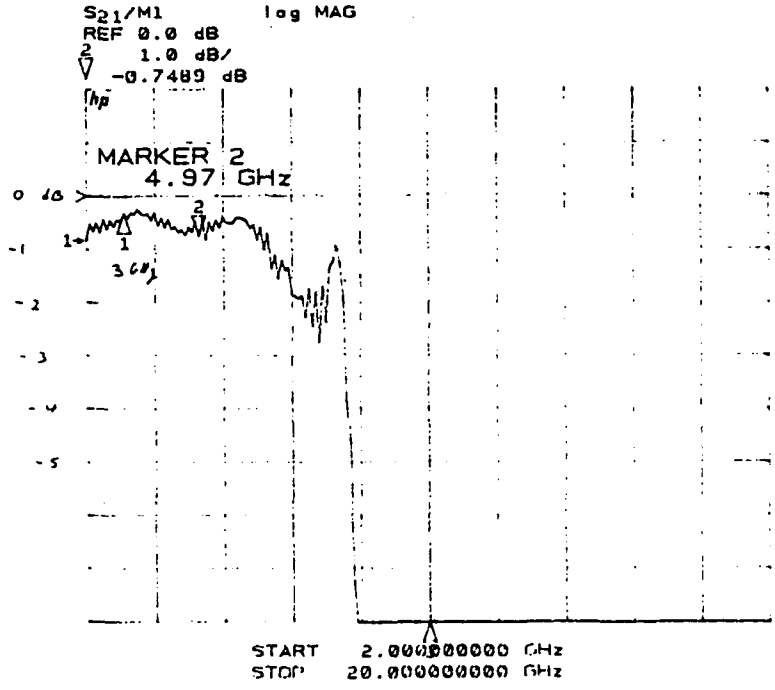


Figure 32. Bandstop filter, insertion loss vs frequency.

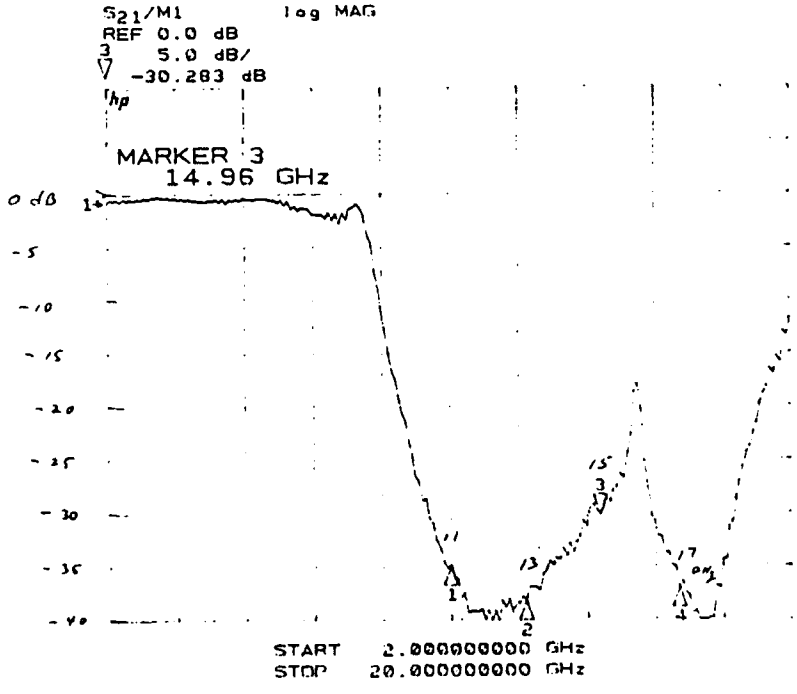


Figure 33. Bandstop filter, attenuation vs frequency.

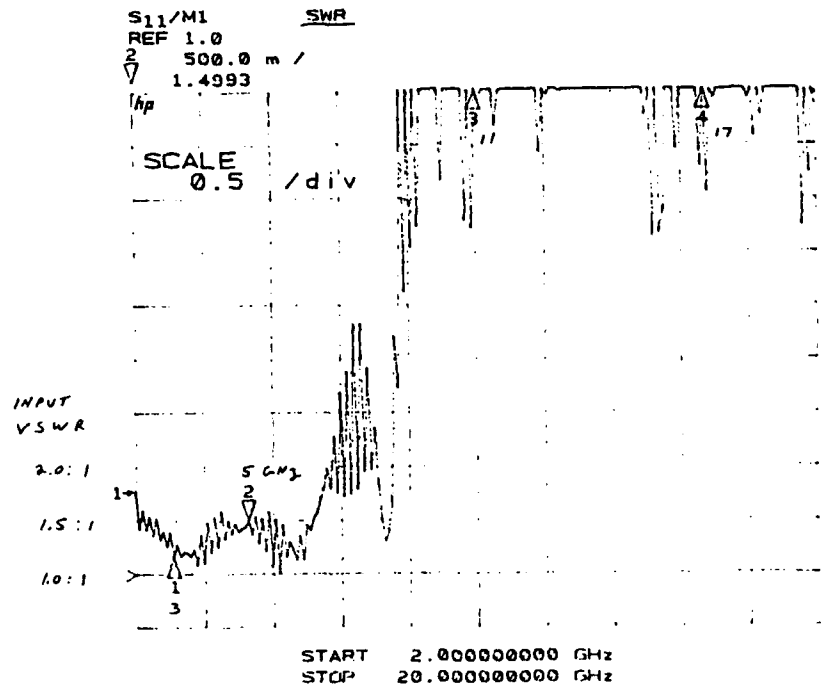


Figure 34. Bandstop filter, VSWR vs frequency.

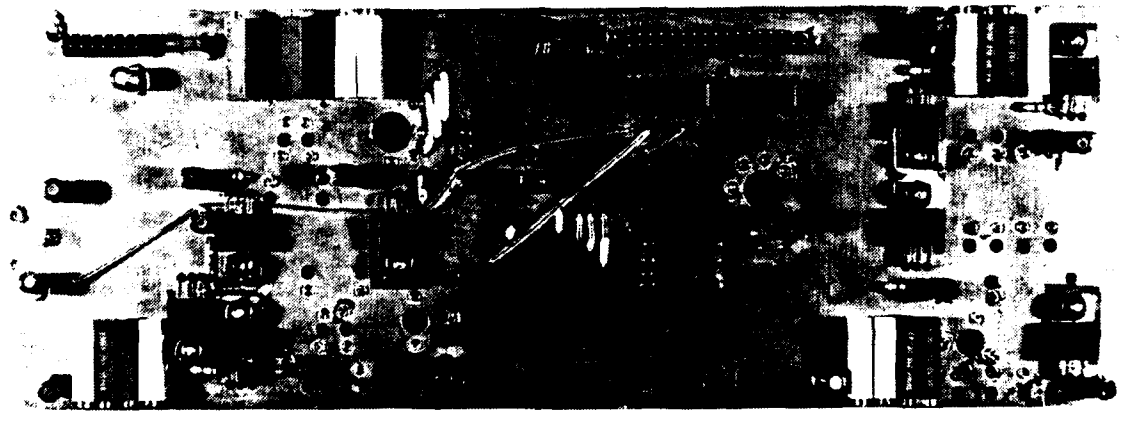


Figure 35. Voltage regulator/switch driver PC Board component side.

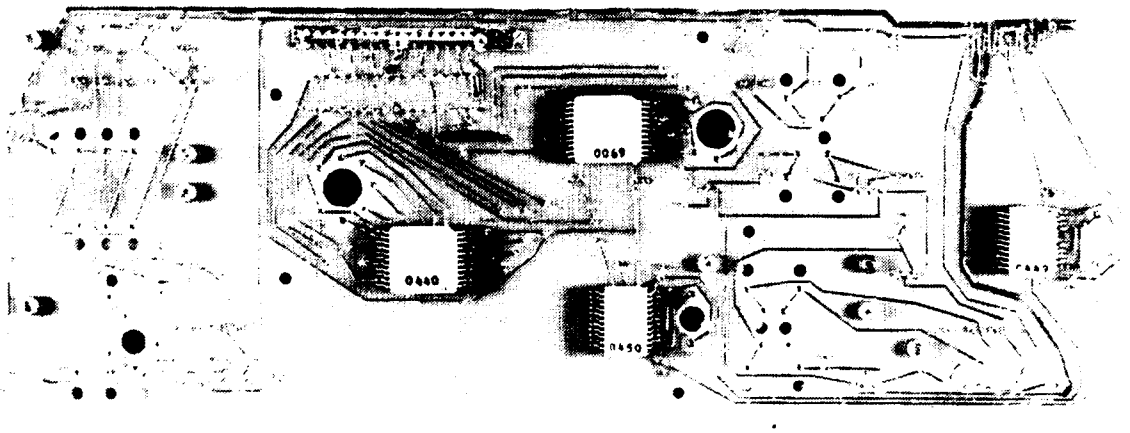


Figure 36. Voltage regulator/switch driver PC Board conductor side.

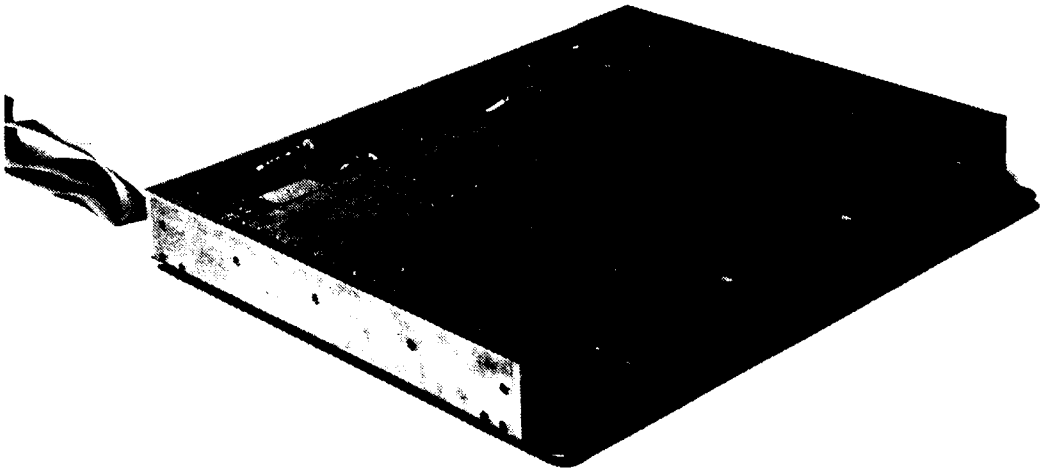


Figure 37. HDRD housing, top cover removed. RF input side.

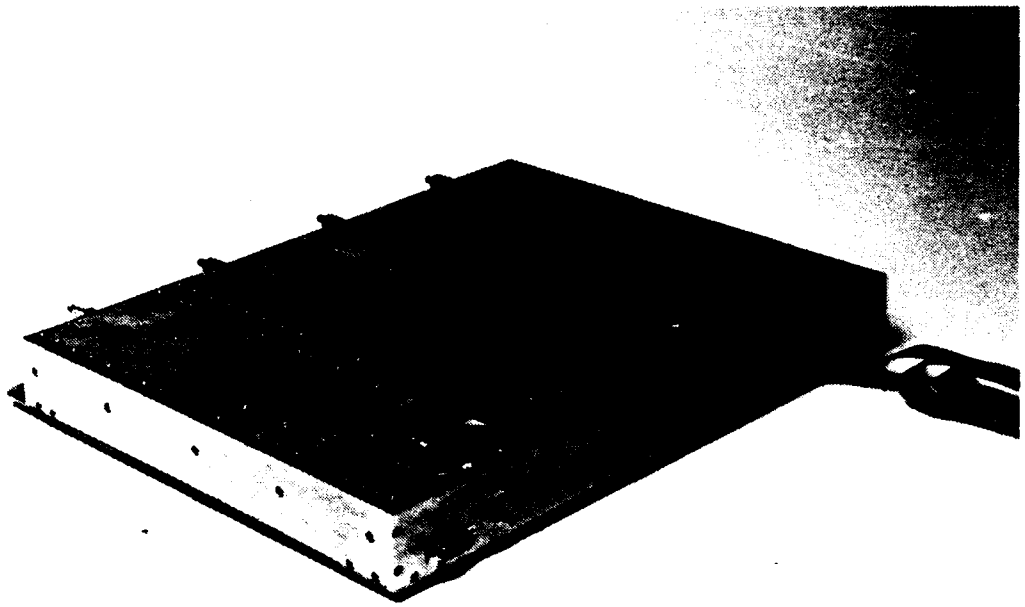


Figure 38. HDRD housing, top cover removed. IF output side.

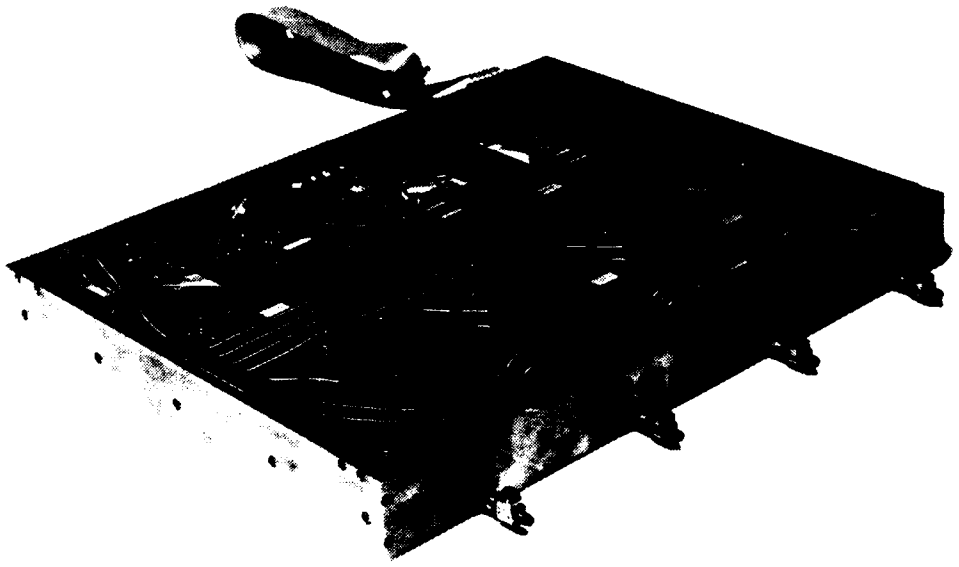


Figure 39. HDRD housing, bottom cover removed. View 1.

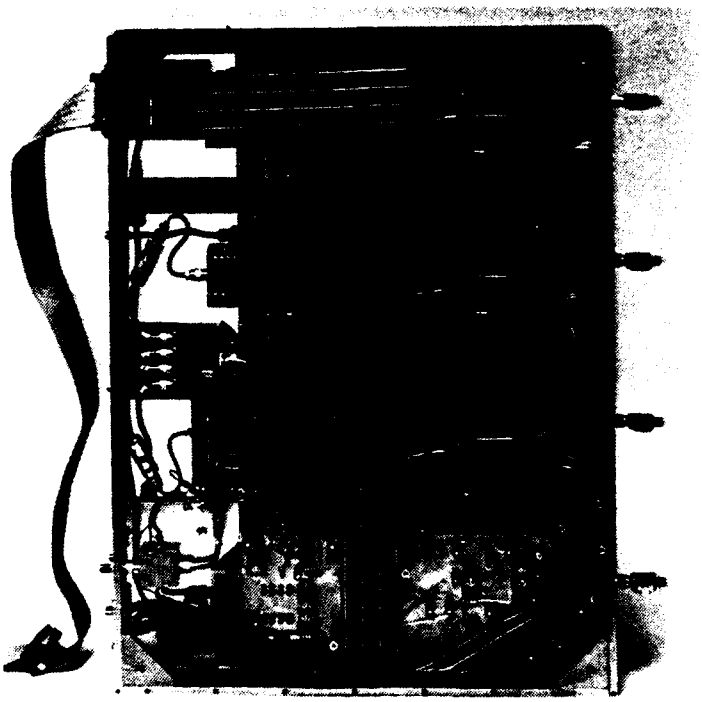


Figure 40. HDRD housing, bottom cover removed. View 2.

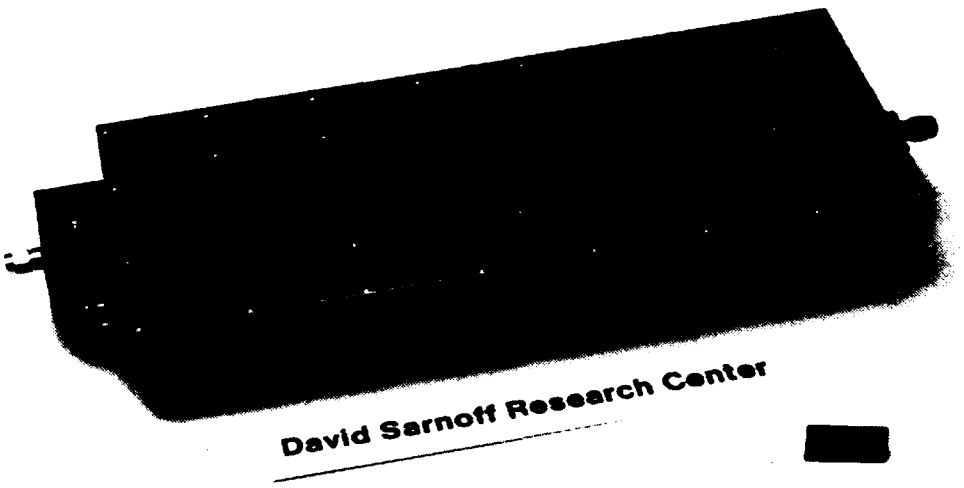


Figure 41. Single downconverter channel, Top view.

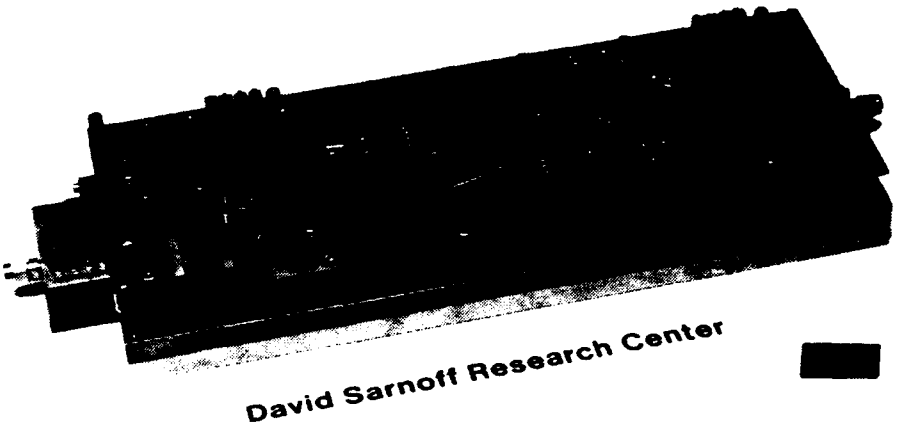


Figure 42. Single downconverter channel, Bottom view.

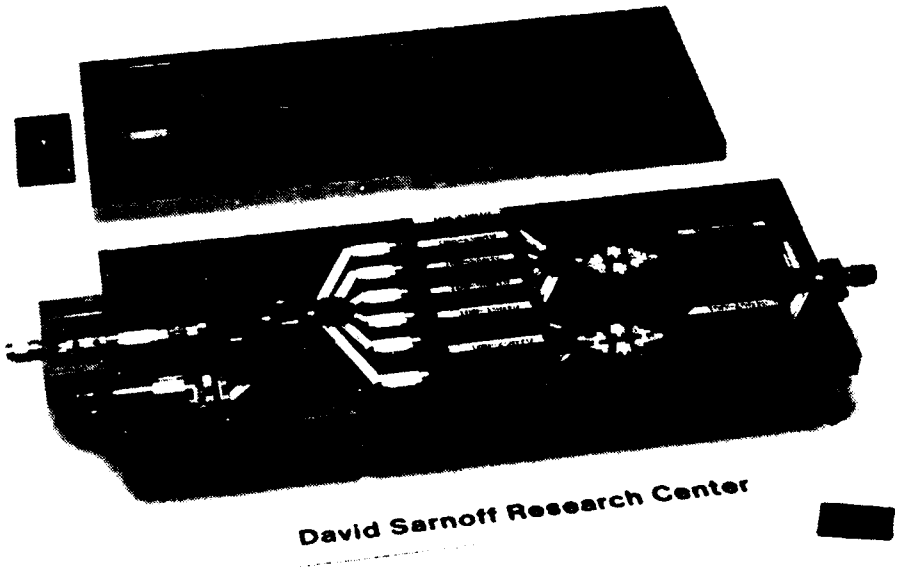


Figure 43. Single downconverter channel, Top view, cover removed.

Section IV

TESTING AND ADJUSTING

The phase tracking among the four channels is the most difficult and critical part of the testing and adjusting of the downconverter. A Hewlett-Packard HP-8510B vector network analyzer (NA) was used in the setup shown in Fig. 44 to measure the tracking of three channels with respect to a fourth, the reference channel. The insertion phase and amplitude of each channel relative to the reference channel was measured and recorded in 10-MHz steps over the full 6- to 18-GHz band. The procedure for doing this was to store the transmission data for the reference channel in the NA data memory and then measure the transmission data for each channel relative to the stored data.

Based on these measured results, the amount of adjustment required is determined and, if necessary, the phase and amplitude trimmers (described in Section III-E) are adjusted and the test repeated.

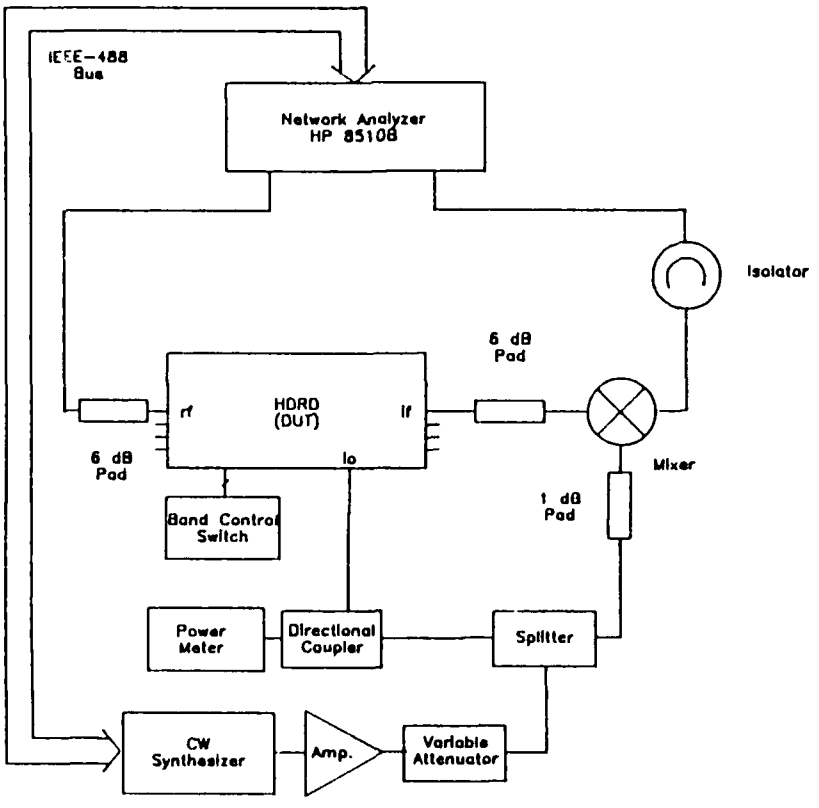


Figure 44. HDRD tracking test set block diagram.

Section V

HDRD PERFORMANCE DATA

A. NOISE FIGURE AND GAIN

A Hewlett-Packard HP 8970S noise figure and gain test set was used to evaluate components of the downconverter as well as the assembled downconverter system channels. A photograph of this test set is shown in Fig. 45. It is capable of measuring noise figure from 10 MHz to 26.5 GHz. In addition to fundamental frequency measurements, this test set also measures the noise figure and gain of frequency conversion devices by first calibrating at the rf input frequency, than calibrating at the IF frequency, and presenting corrected data. The noise figure and gain of each channel was measured and recorded over each subband at 100-MHz intervals. The plotted data for each subband of the HDRD are shown in Appendix A.

B. THIRD-ORDER INTERCEPT POINT

The third-order intercept point test set automatically measures the two-tone, third-order intercept point and stores the data in a computer file. A block diagram of this test set is shown in Fig. 46. The test set uses an HP 8566B Spectrum Analyzer to measure the frequency and signal level of the two fundamental tones and the spurious products that they generate in the device under test. The two tones used in the test are generated by two HP 8350B signal generators that operate over the 0.01- to 20-GHz frequency range.

This test set was used to evaluate downconverter components and to test the performance of each channel of the downconverter system. The third-order intercept point of the downconverter system was measured at three frequencies in each subband with the fundamental tones separated by 10 MHz and the results recorded.

Figure 47 shows the two-tone, spur-free dynamic range vs frequency of a typical channel.

C. LINEAR DYNAMIC RANGE

The linear dynamic range is a single-tone test in which the input signal level is increased until the 1-dB compression point of the downconverter is reached. The difference between output power at the 1-dB compression point, in dBm, and the calculated system-output noise floor in a 50-MHz bandwidth is the linear dynamic range. The noise floor is:

$$NFl = kT + 10LogBW + gain + noise\ figure,$$

where, kT = -114 dB/MHz, BW = pre-detection bandwidth in MHz, and the gain and noise figure are the previously measured values, in dB.

A plot of the measured linear-dynamic range for all four channels is shown in Fig. 48.

D. PHASE AND AMPLITUDE TRACKING

The phase and amplitude tracking of each channel was measured and recorded over each subband in 10-MHz intervals. The plotted data for each subband of the HDRD are shown in Appendix B.

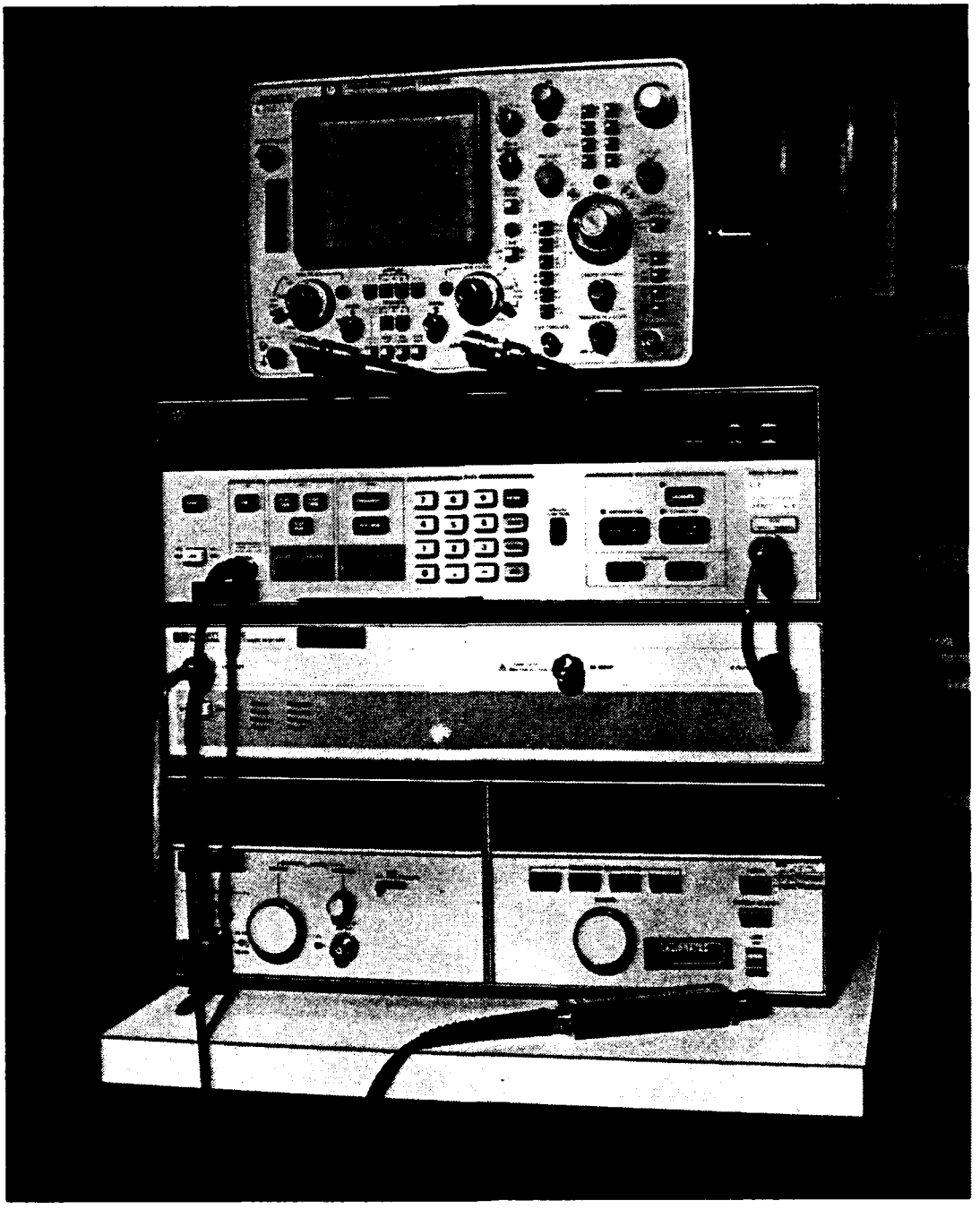


Figure 45. Noise figure and gain test set.

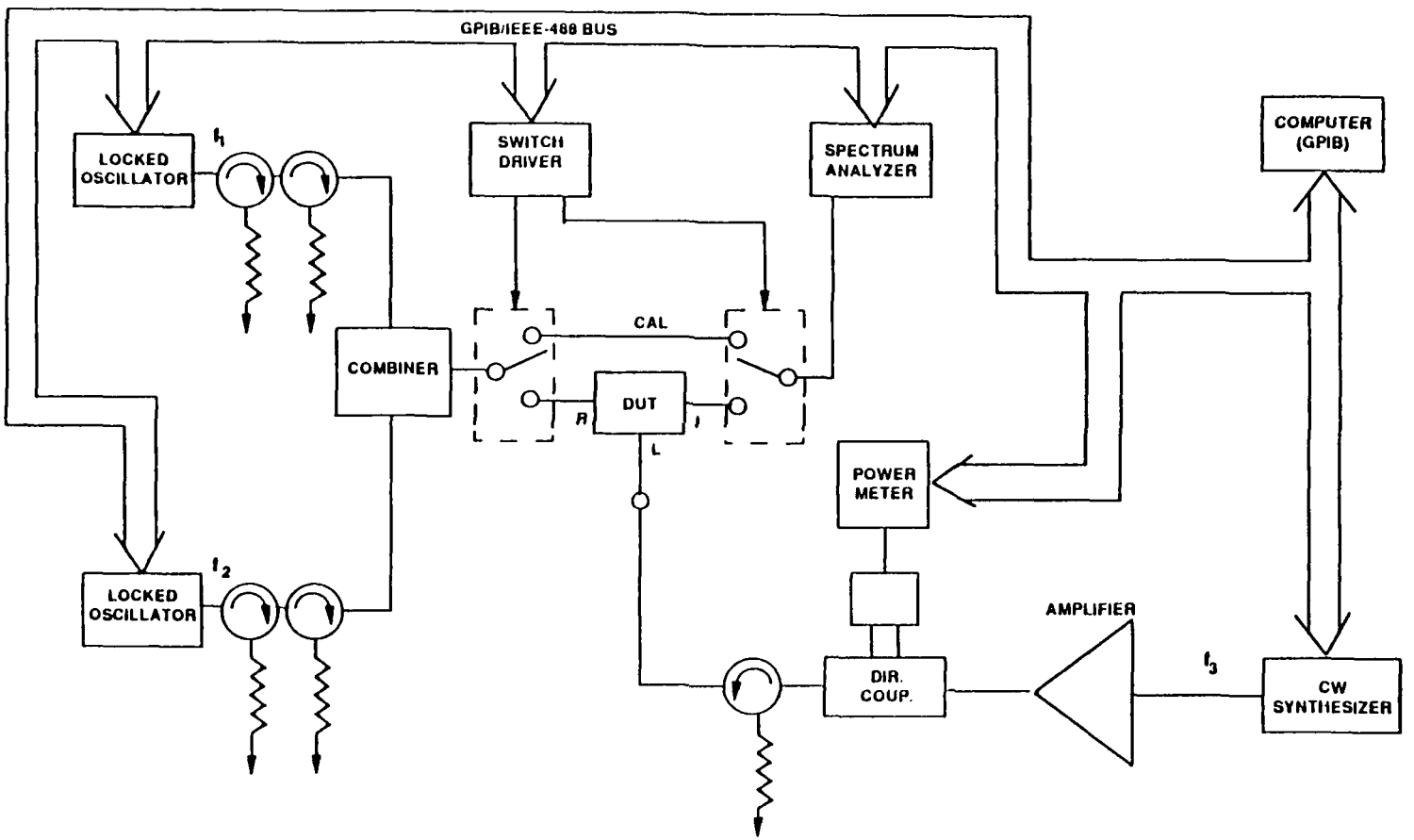


Figure 46. Third-order intercept point test set.

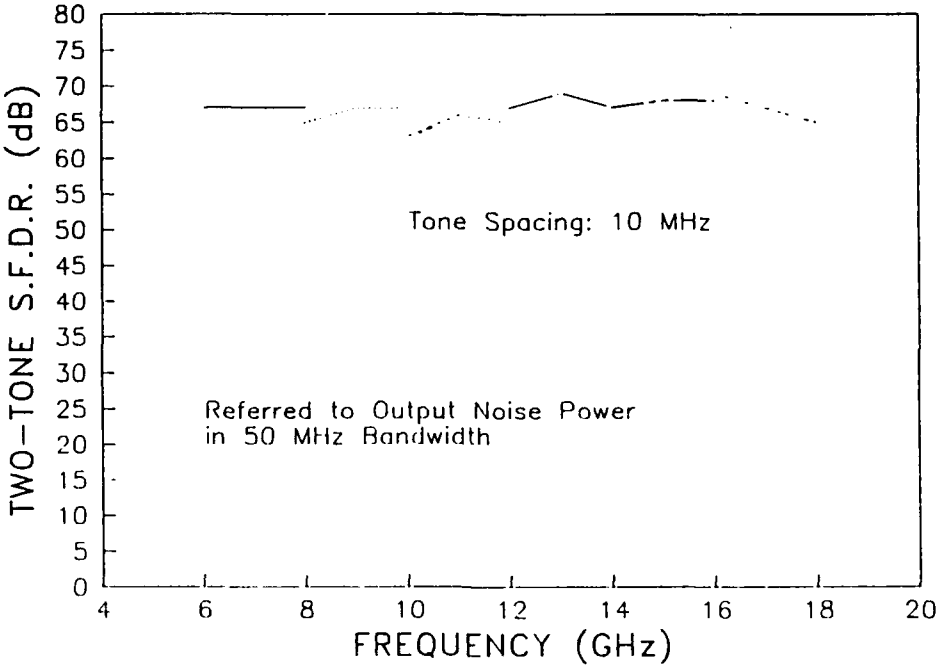


Figure 47. Two-tone, spur-free, dynamic range vs frequency.

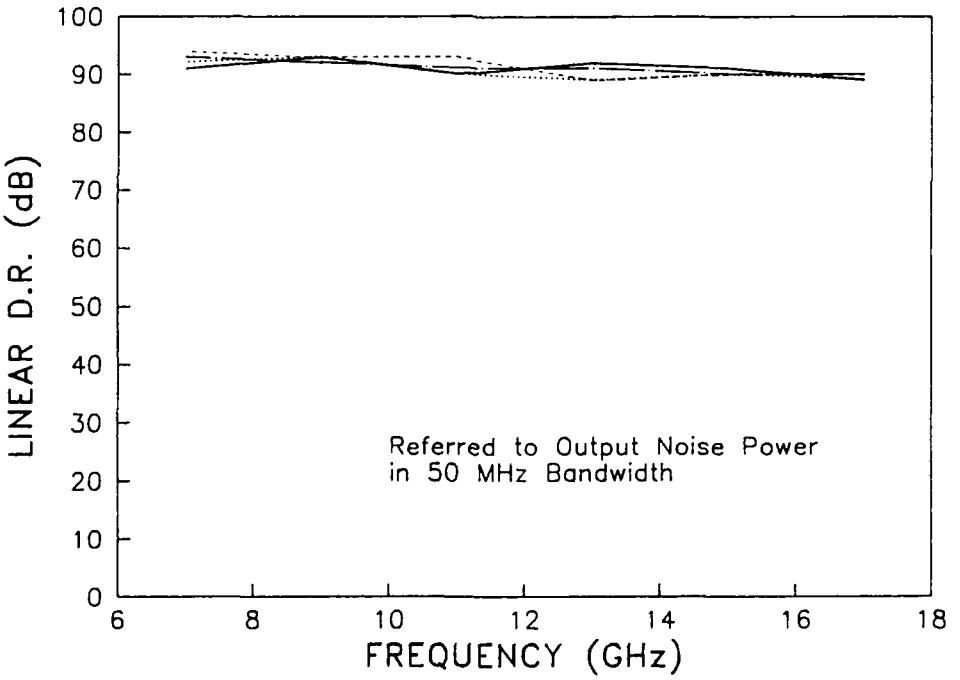


Figure 48. Linear, spur-free, dynamic range vs frequency.

Section VI

CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

The HDRD achieved excellent performance with a SFDR of 65 dB, and a linear dynamic range of 90 dB, in a predetection bandwidth of 50 MHz. These results were due to the following key features:

- Use of wideband, low-noise, and high-intercept point MMIC amplifiers
- Use of low-loss series/shunt PIN switches
- Low-loss filters and diplexers
- Use of a high-dynamic-range mixer

Problems were encountered with excessive phase- and amplitude-ripple due to mismatches of the commercial coaxial filters inserted in a microstrip circuit. In addition, some of the critical components were not amplitude- and phase-matched at the manufacturer's location. This contributed to problems in achieving good phase and amplitude matching between channels over the complete 6- to 18-GHz band.

B. RECOMMENDATIONS

1. Integrate switches and amplifiers.
2. Assemble each channel in a modular format where each major function is a separate, testable, and adjustable module.
3. Test every subcomponent and adjust it to meet tighter VSWR, gain flatness, and phase- and amplitude-tracking requirements.
4. Minimized the number of coaxial-to-microstrip transitions to keep mismatches to a minimum.
5. Implement a subcomponent grounding technique that provides the shortest and most consistent path to ground.
6. Assemble and inspect subassemblies under the surveillance of the Quality Assurance department.

7. Modularize the downconverter so that adjustments and repairs are readily and efficiently accomplished and, where necessary, entire tested modules can be exchanged for defective ones.
8. Separate the power supply/regulation function from the rf modules, instead of PC boards with voltage regulators mounted on each channel, so that the removal of a simple multi-pin connector is all that will be required prior to rf module repair.
9. Add a voltage sequencer, which ensures that the negative gate voltage to all of the amplifiers is turned on first and off last, regardless of the actual sequence of the input voltages.
10. Redesign and repackage the downconverter using lighter weight materials and a more compact circuit layout.

REFERENCES

1. Tsui, James B., *Microwave Receivers with Electronic Warfare Applications,* New York, John Wiley & Sons, 1986.

2. Erst, Stephen J., *Receiving Systems Design.* Dedham, MA: Artech House, 1984.

Appendix A

Noise and Gain Data

Appendix A

Noise Figure and Gain Data

The following pages are the plots of the noise figure (NF) and gain of each subband of each channel of the HDRD. The left scale is the NF with the triangle marking the NF plot. The right scale shows the gain with its plot marker. The page sequence is by subband frequency first, then by channel. The HP8970S noise figure and gain test set used to measure this performance is shown in Fig. A-1.

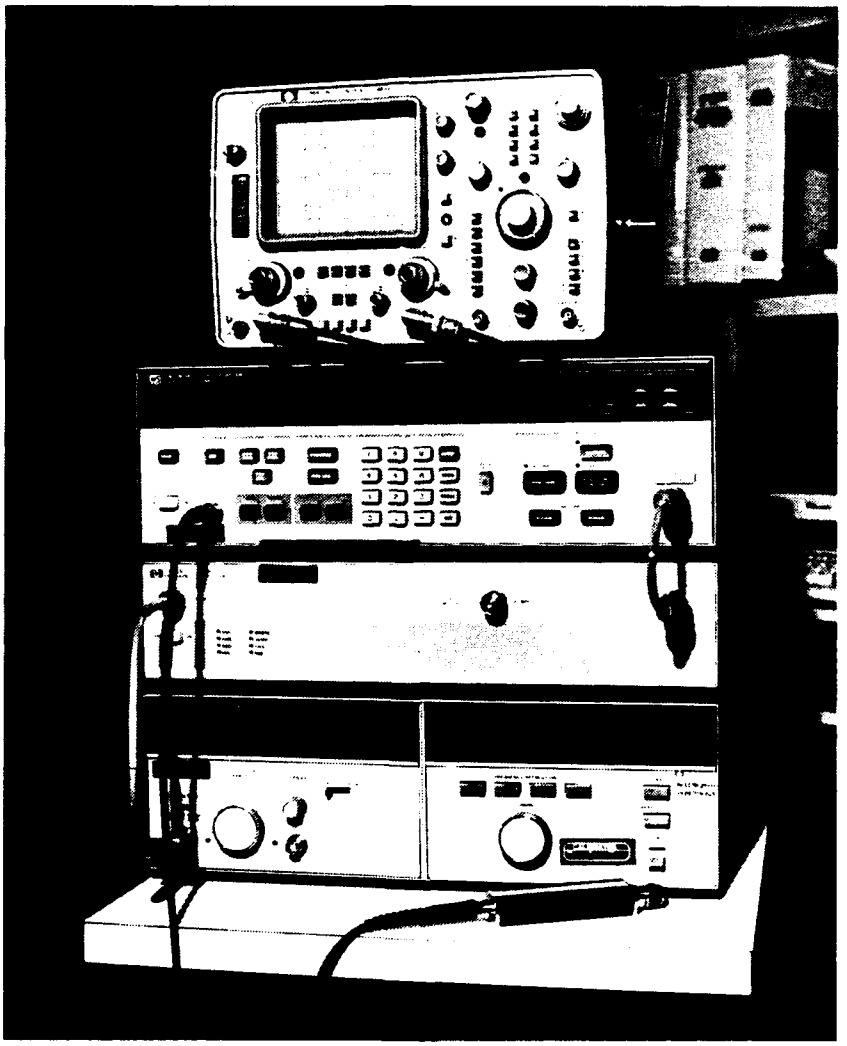
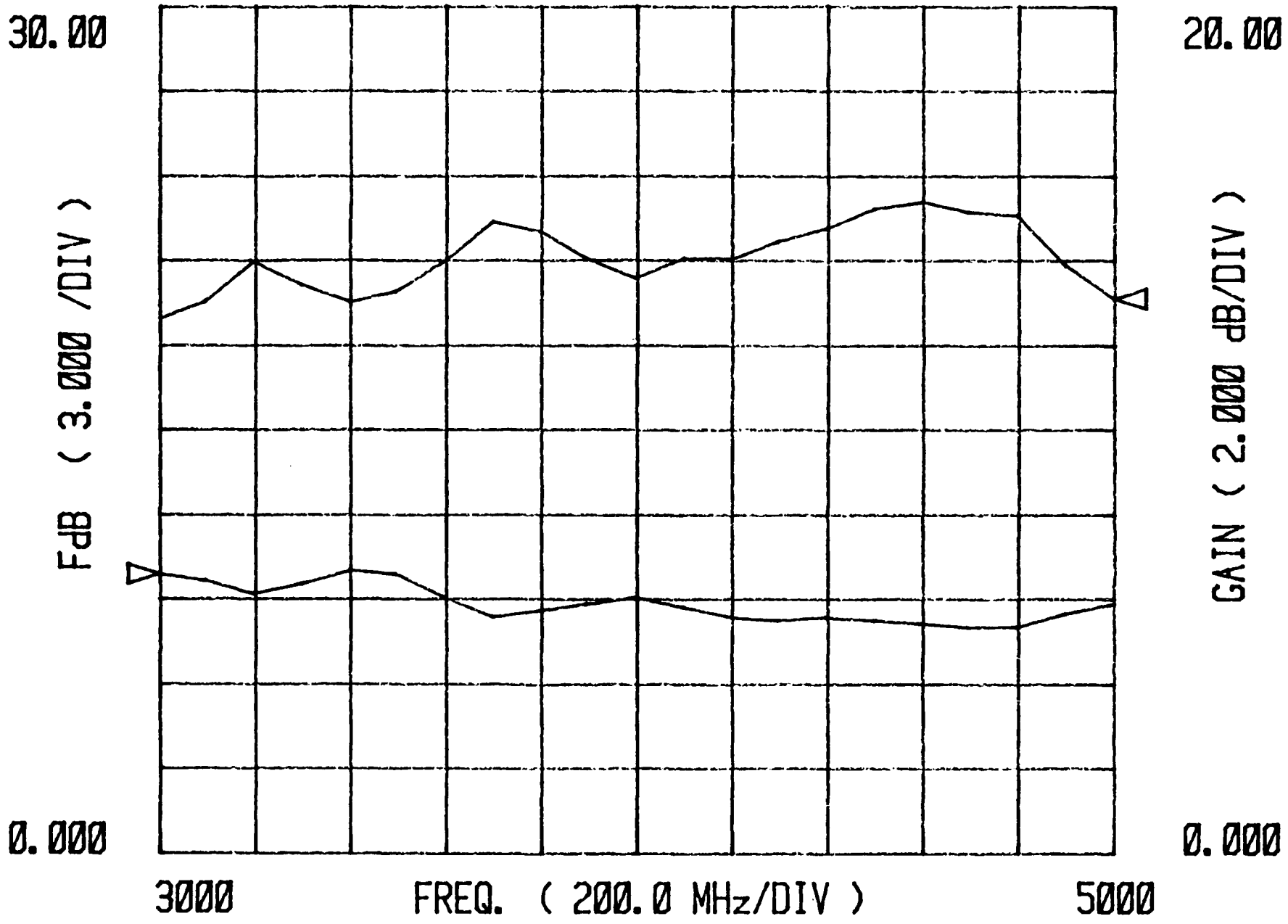
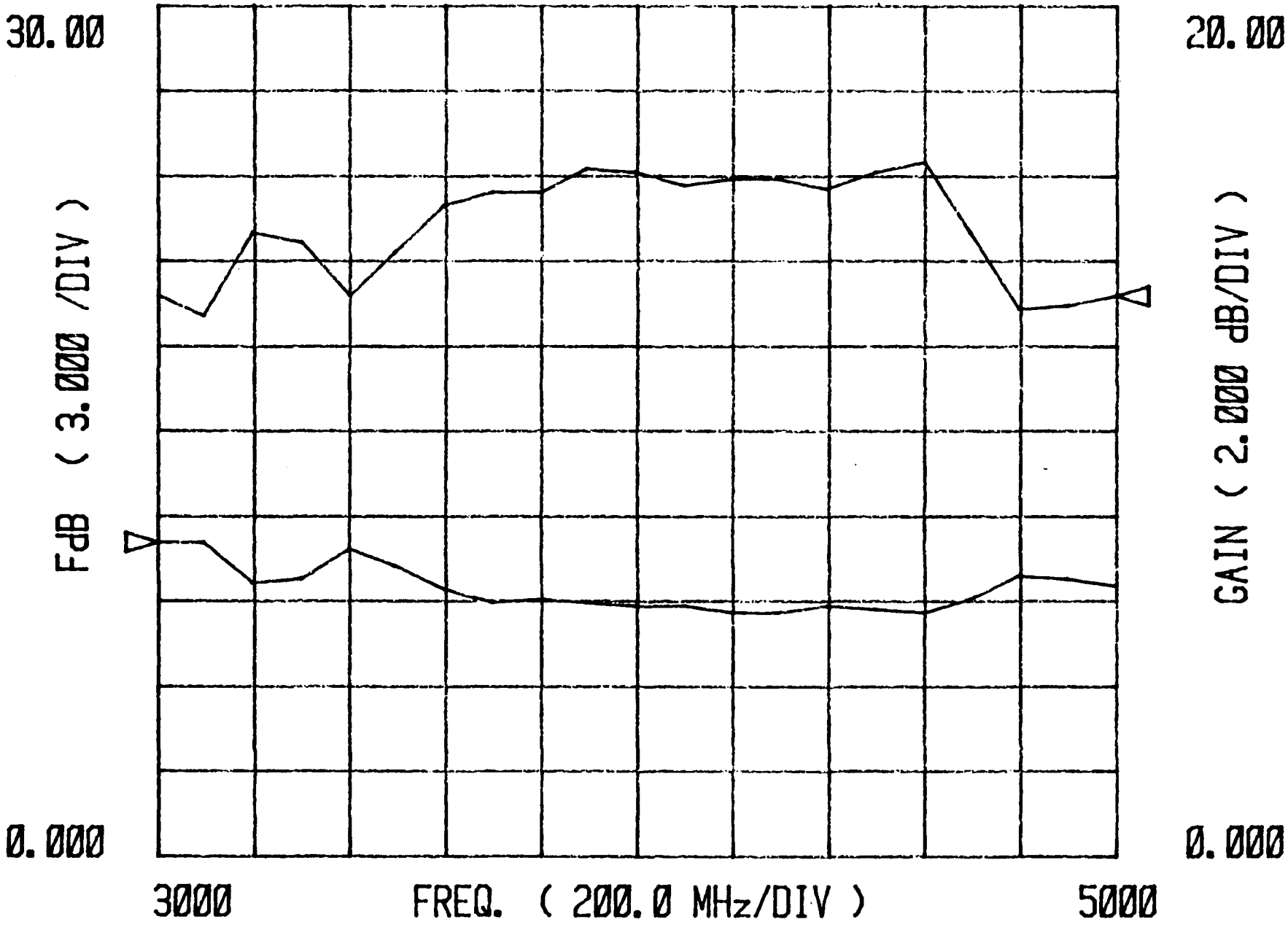


Figure A-1. Noise figure and gain test set.

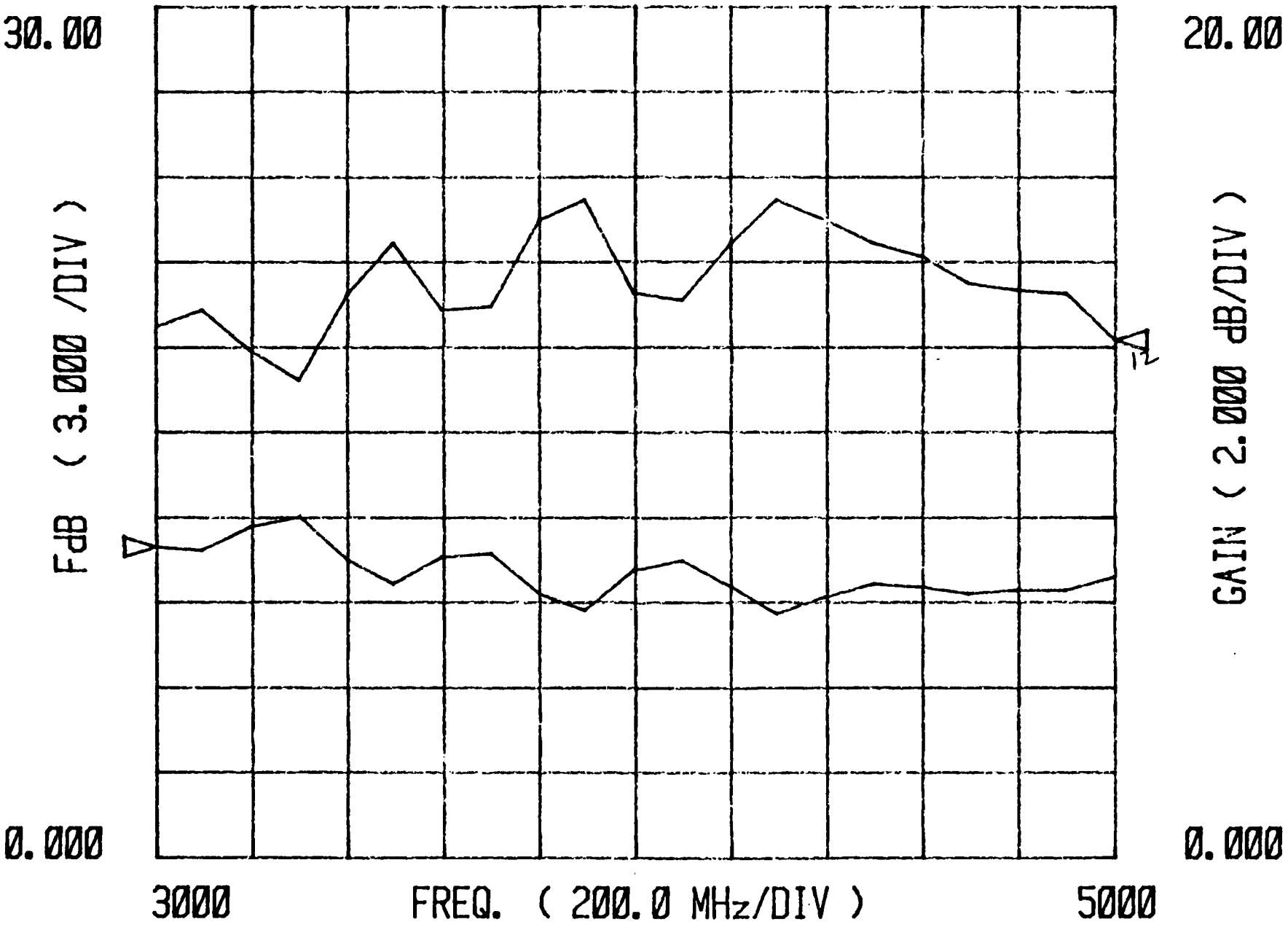
7/13/71
RF 6-8 GHz
CHAN 1



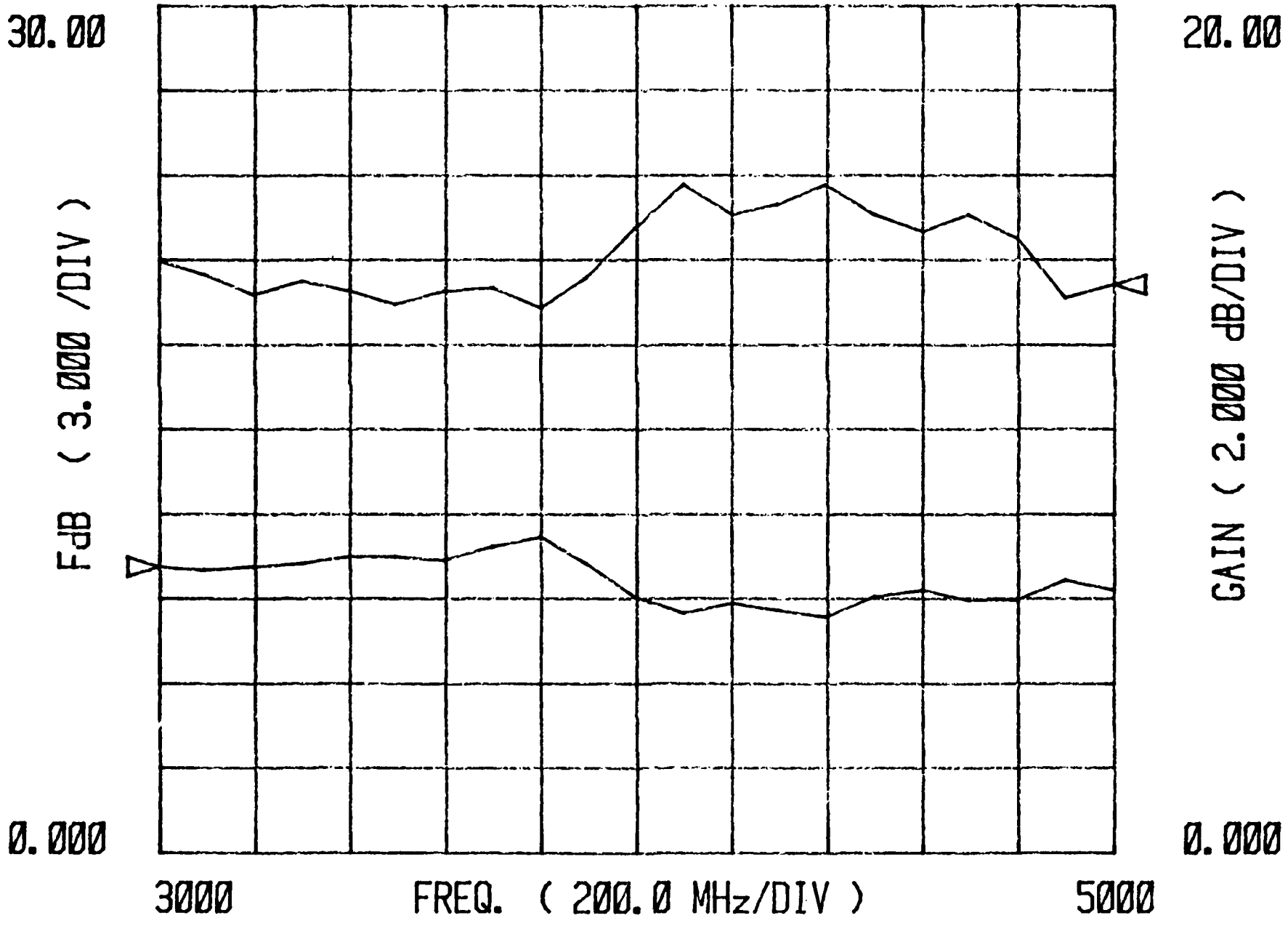
4/2/11
RF 6-8 GHz
CHAN 2



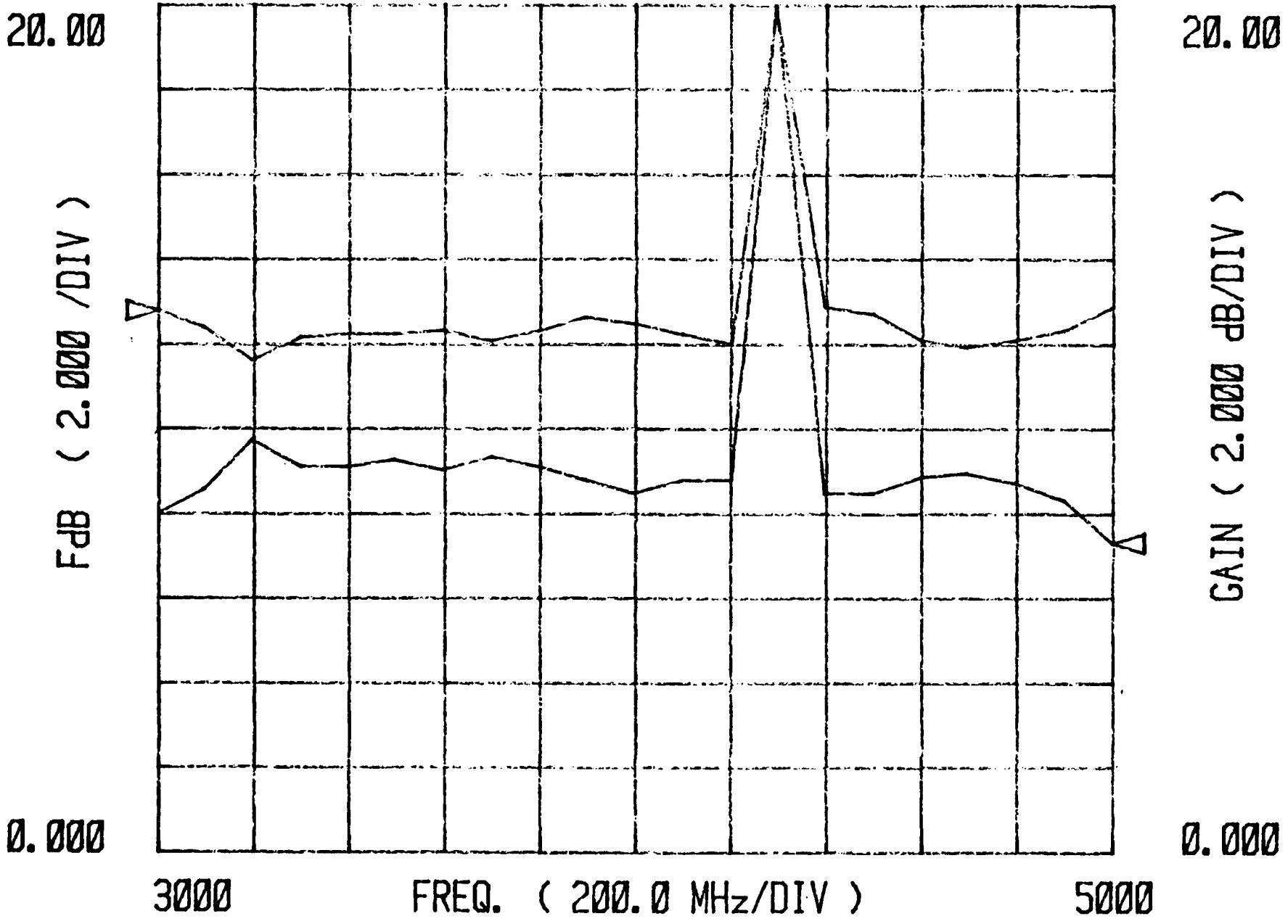
4/13/91
RF 6-8GHz
CHAN 3



4/12/71
RF 6-8GHz
CHAN 4



4/2/11
RF 8-10 GHz
CHAN 1



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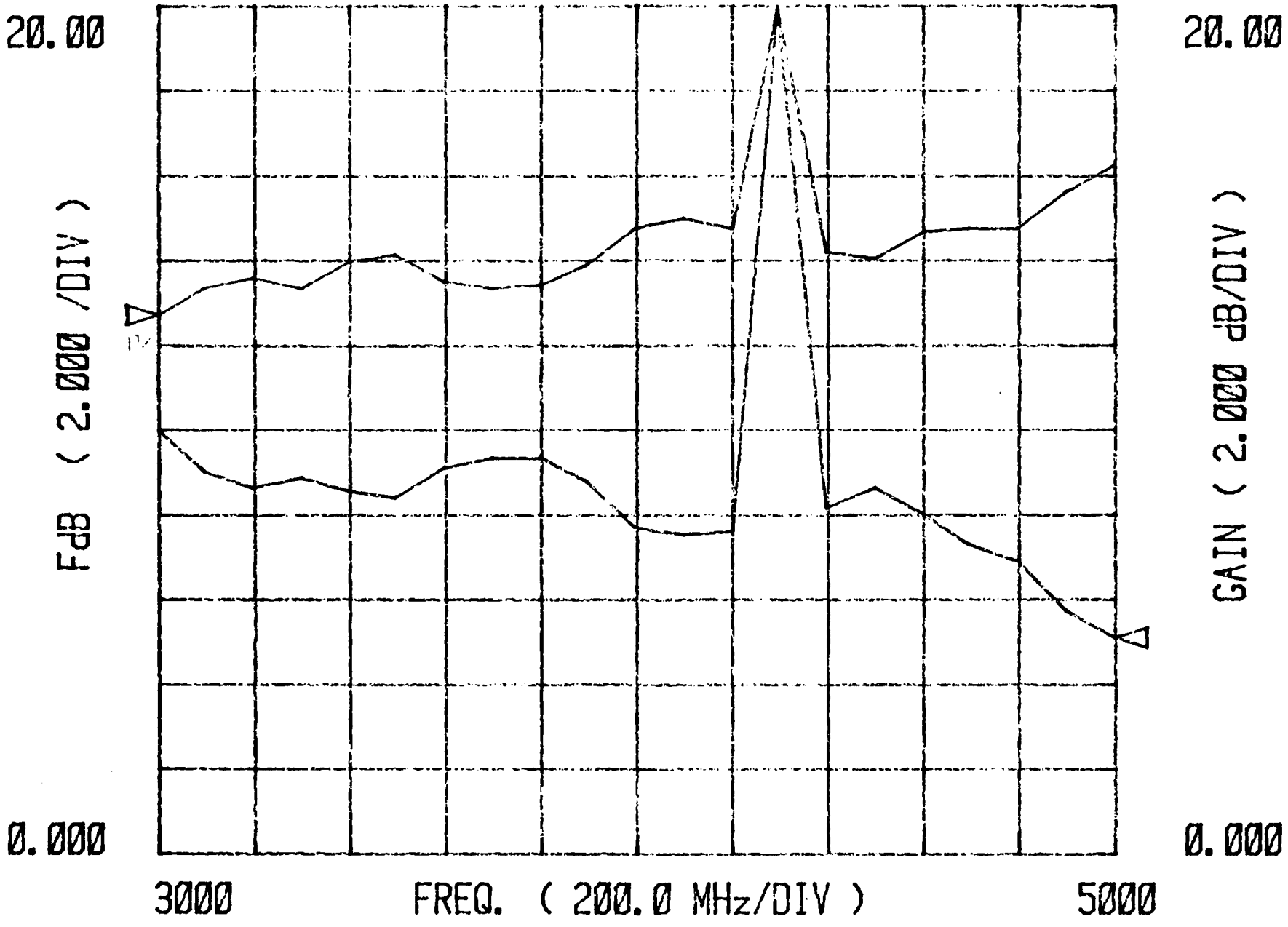
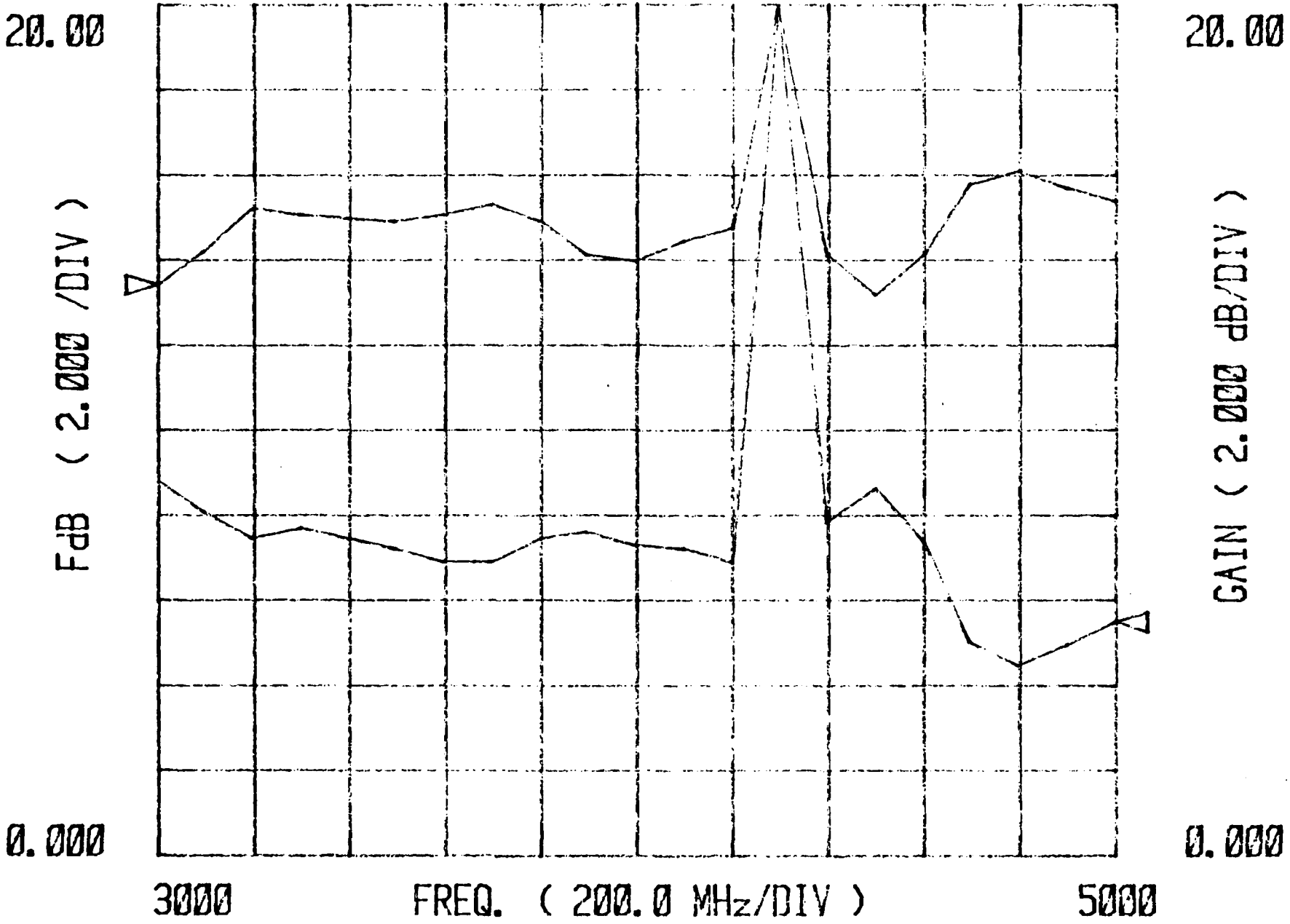
RF 8-10 GHz
CHAN 2



4/17/11
RF 8-10 GHz
CHAN 3



RF 8-10GHz
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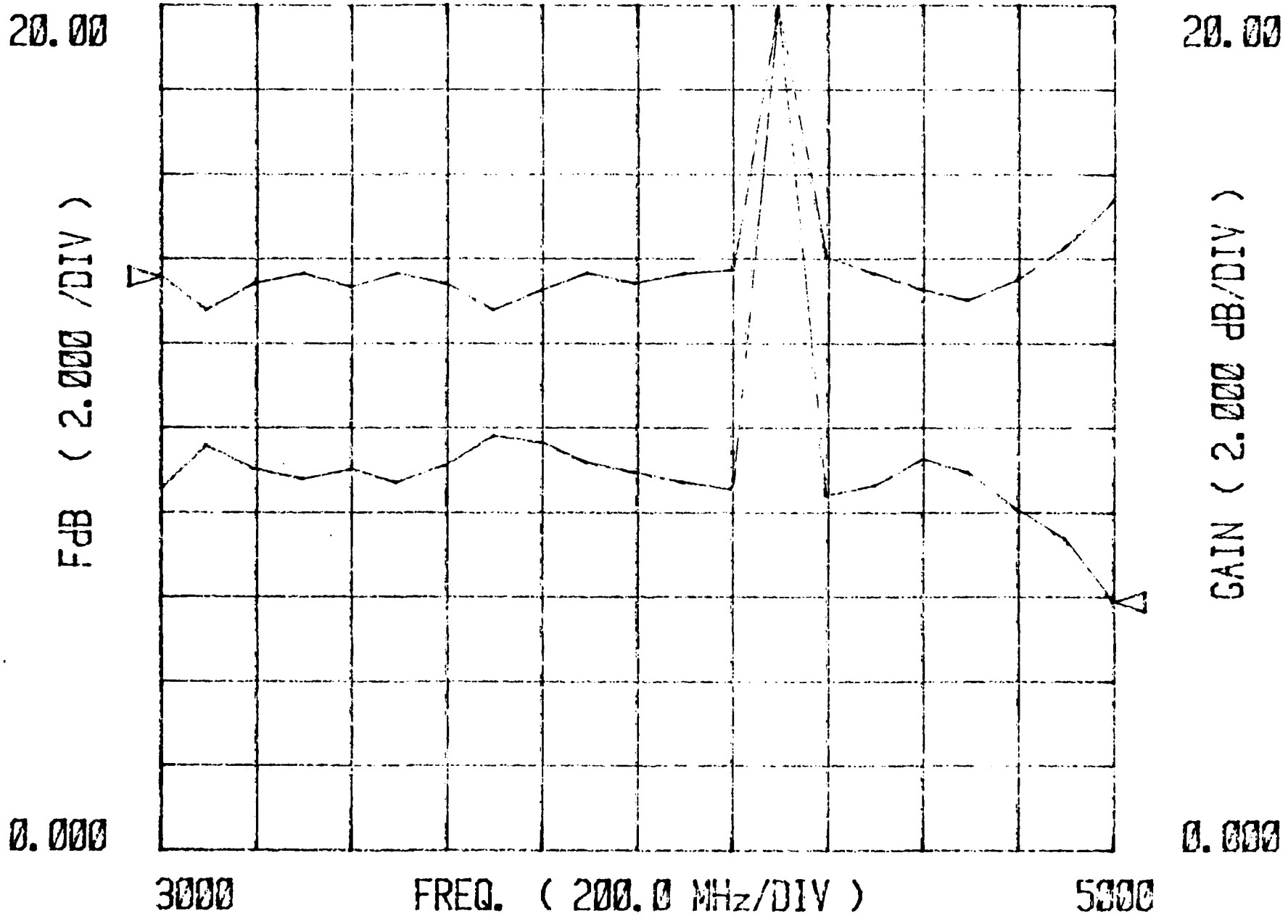

4/13/11
RF 10-12 GHz
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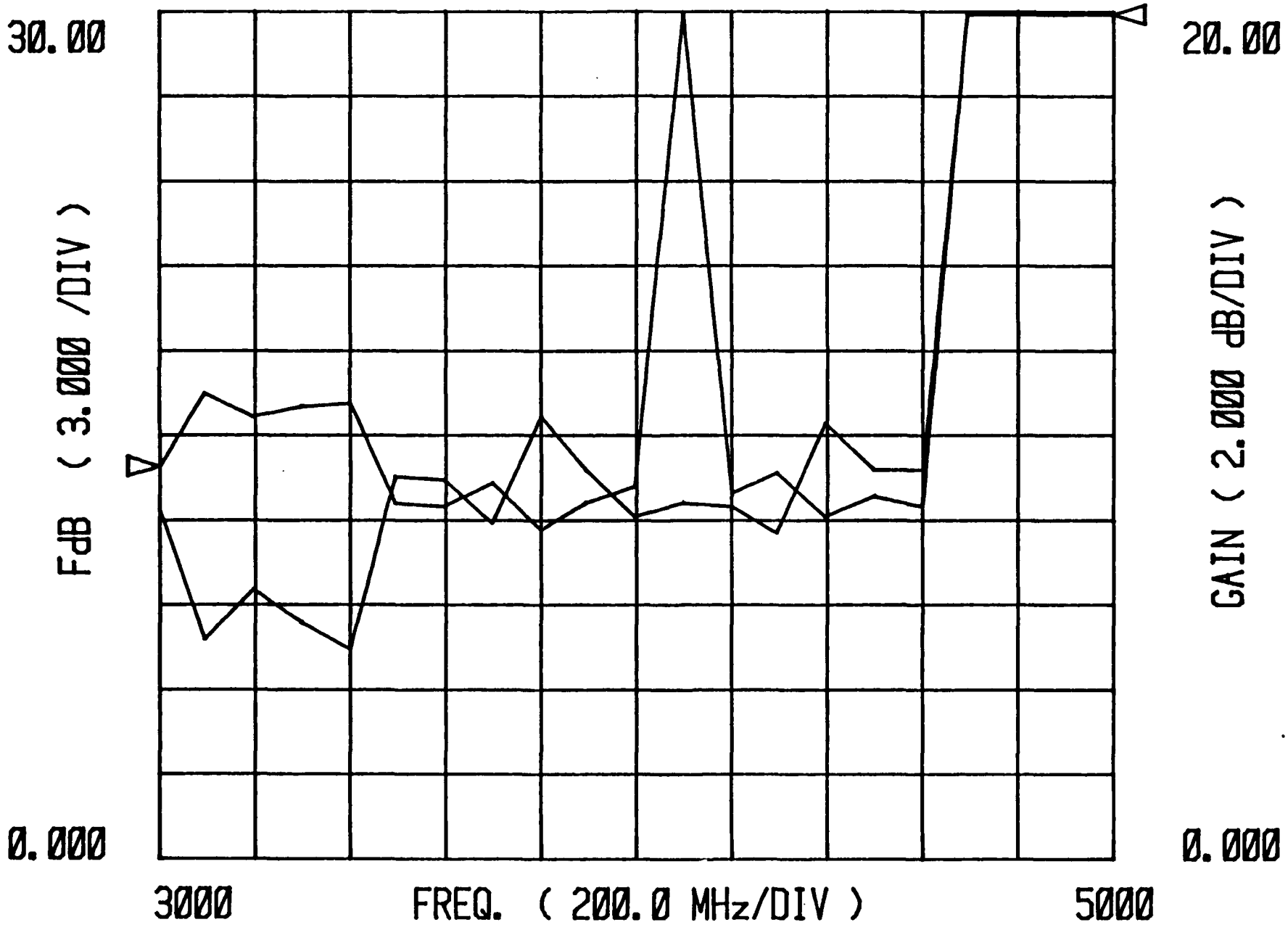
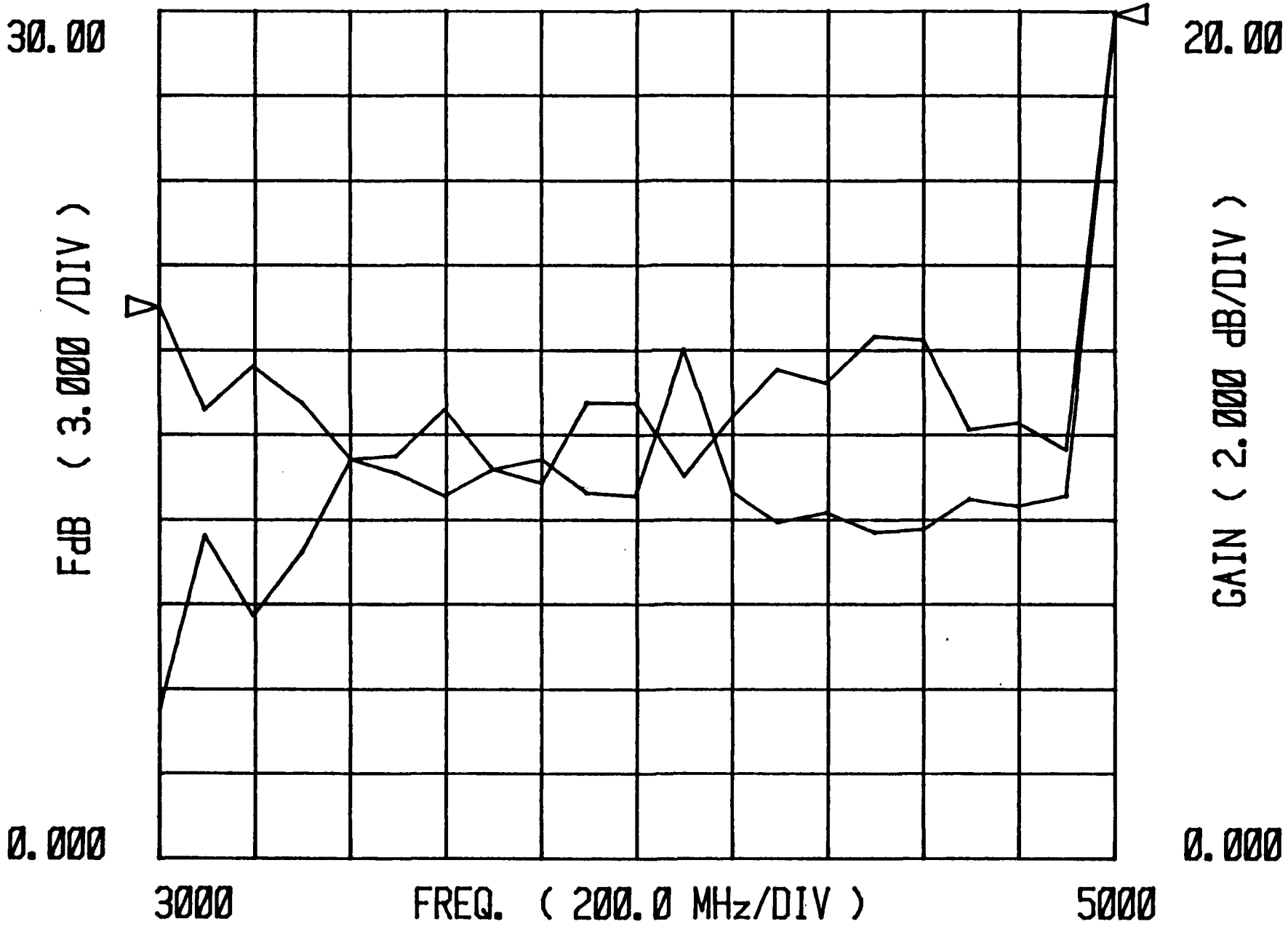
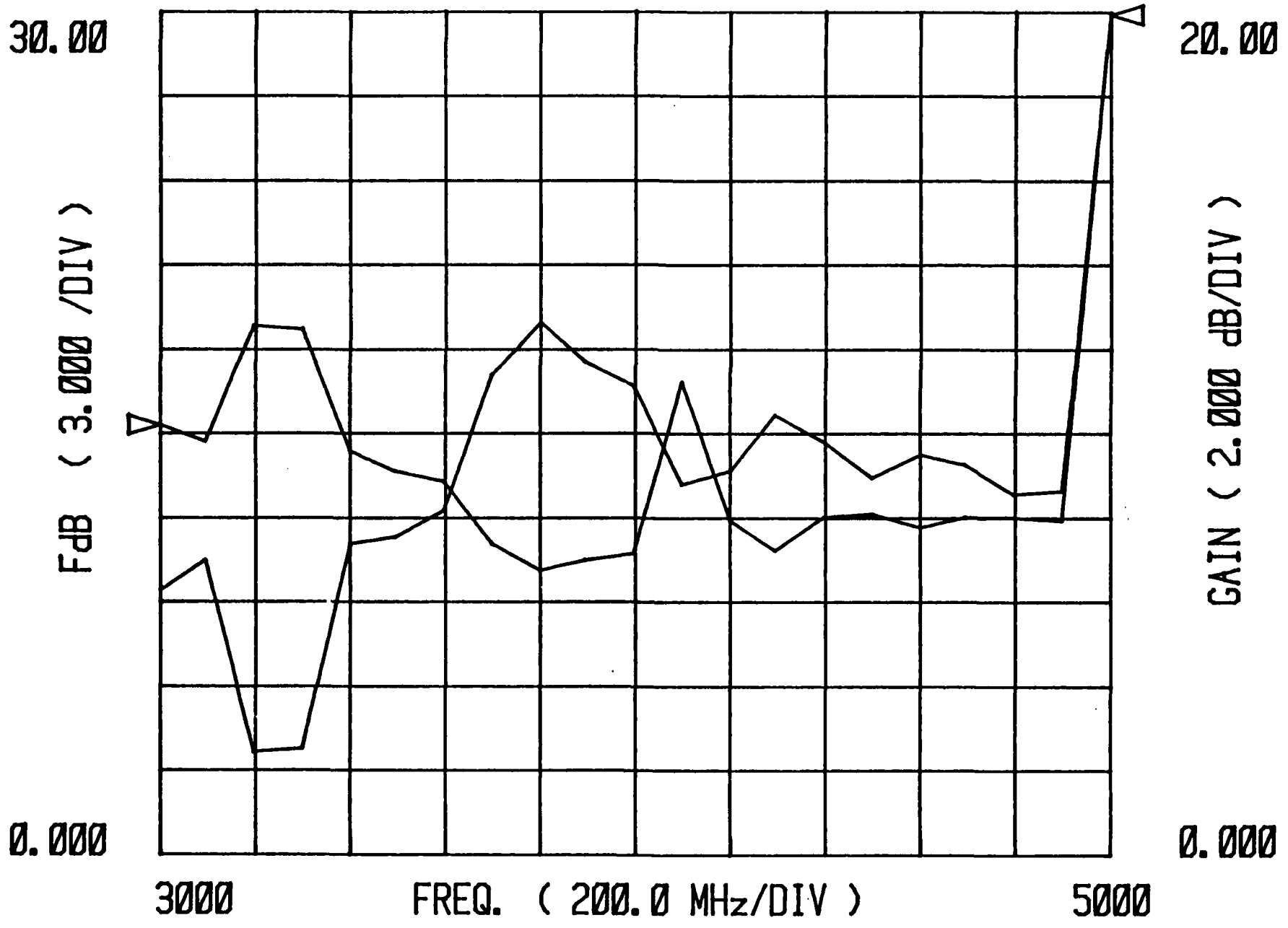


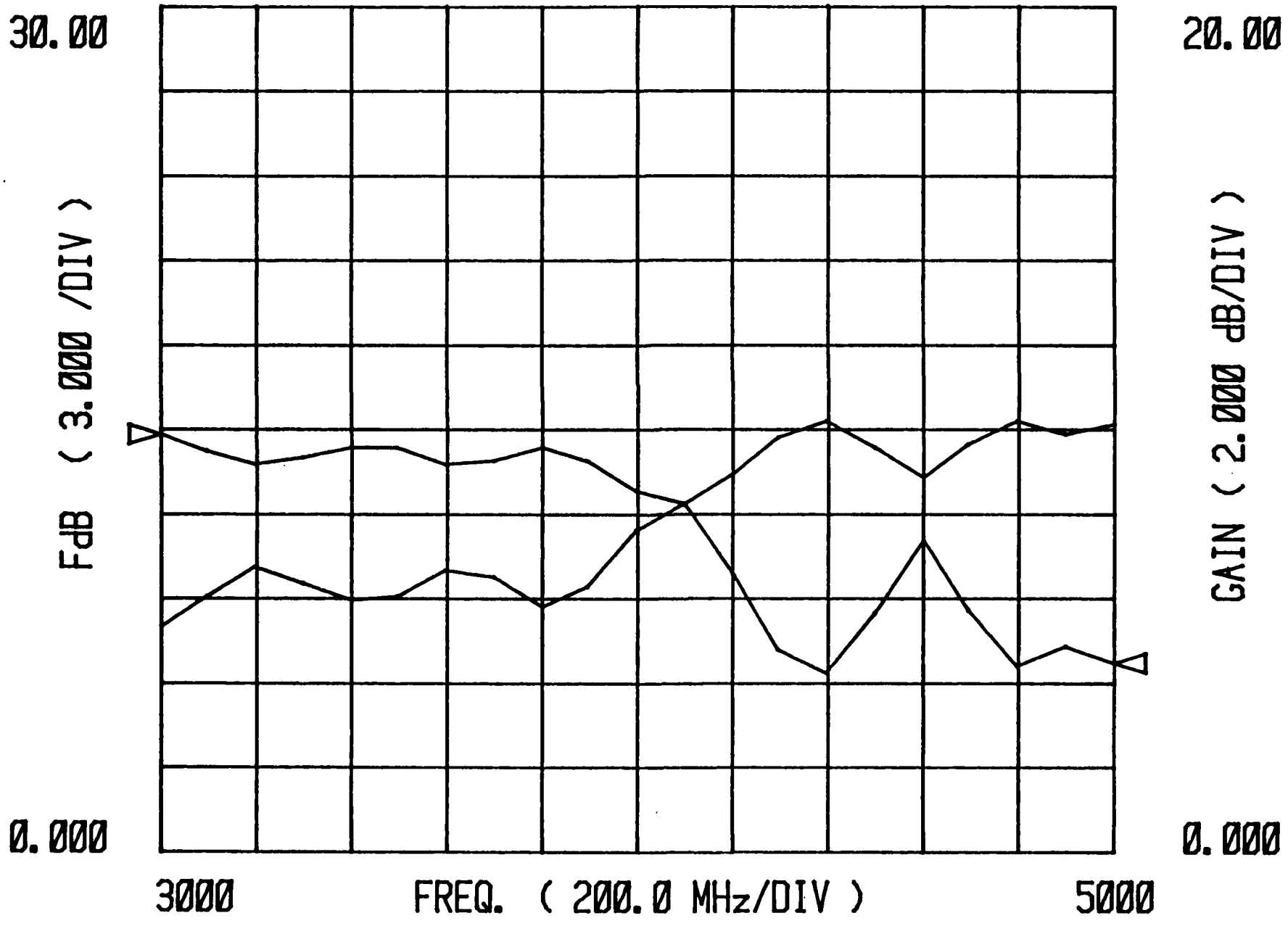
4/12/71
RF 10-12 GHz
CHAN 2



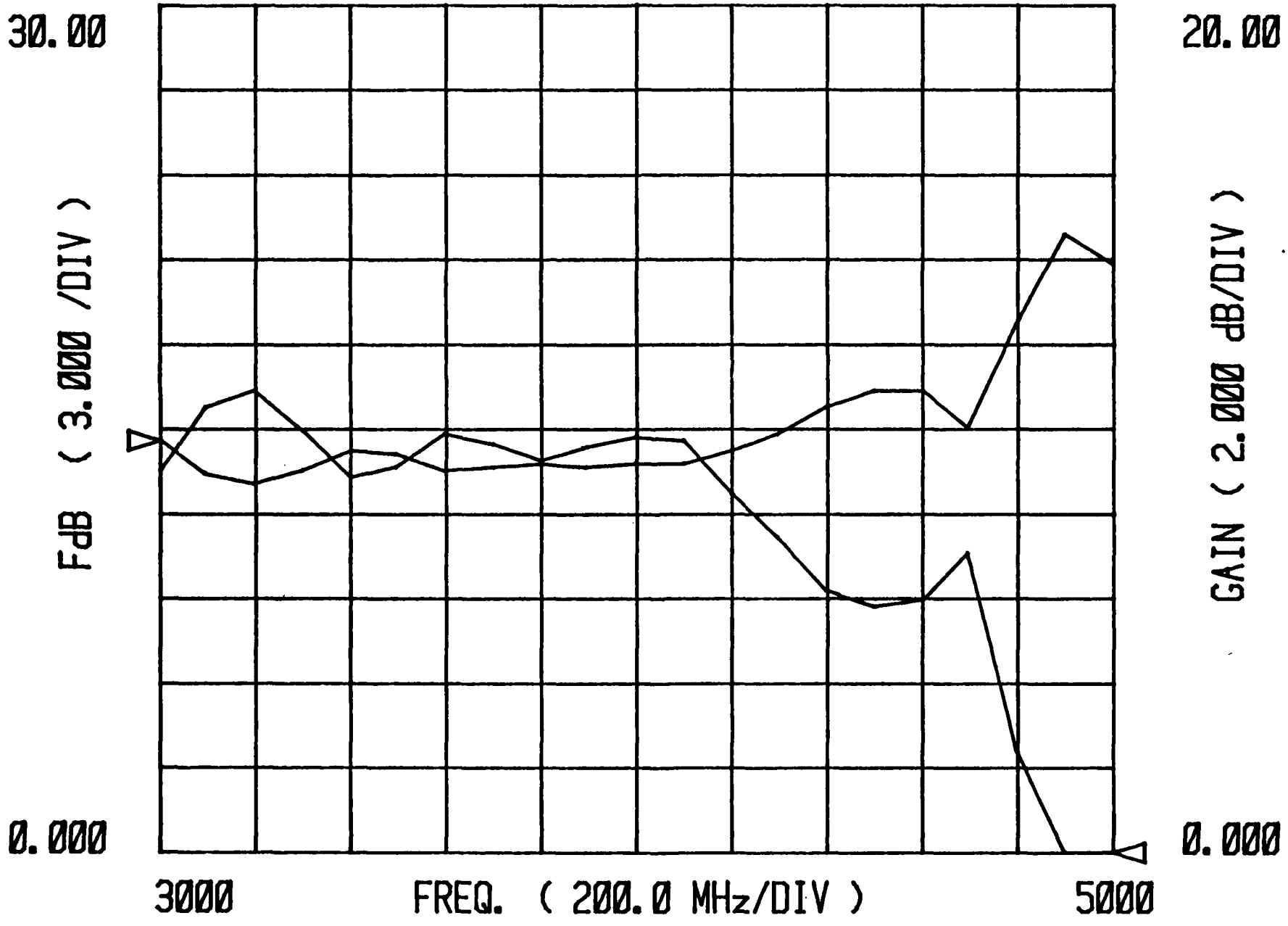
2/13/91
RF 10-12 GHz
CHAN 3



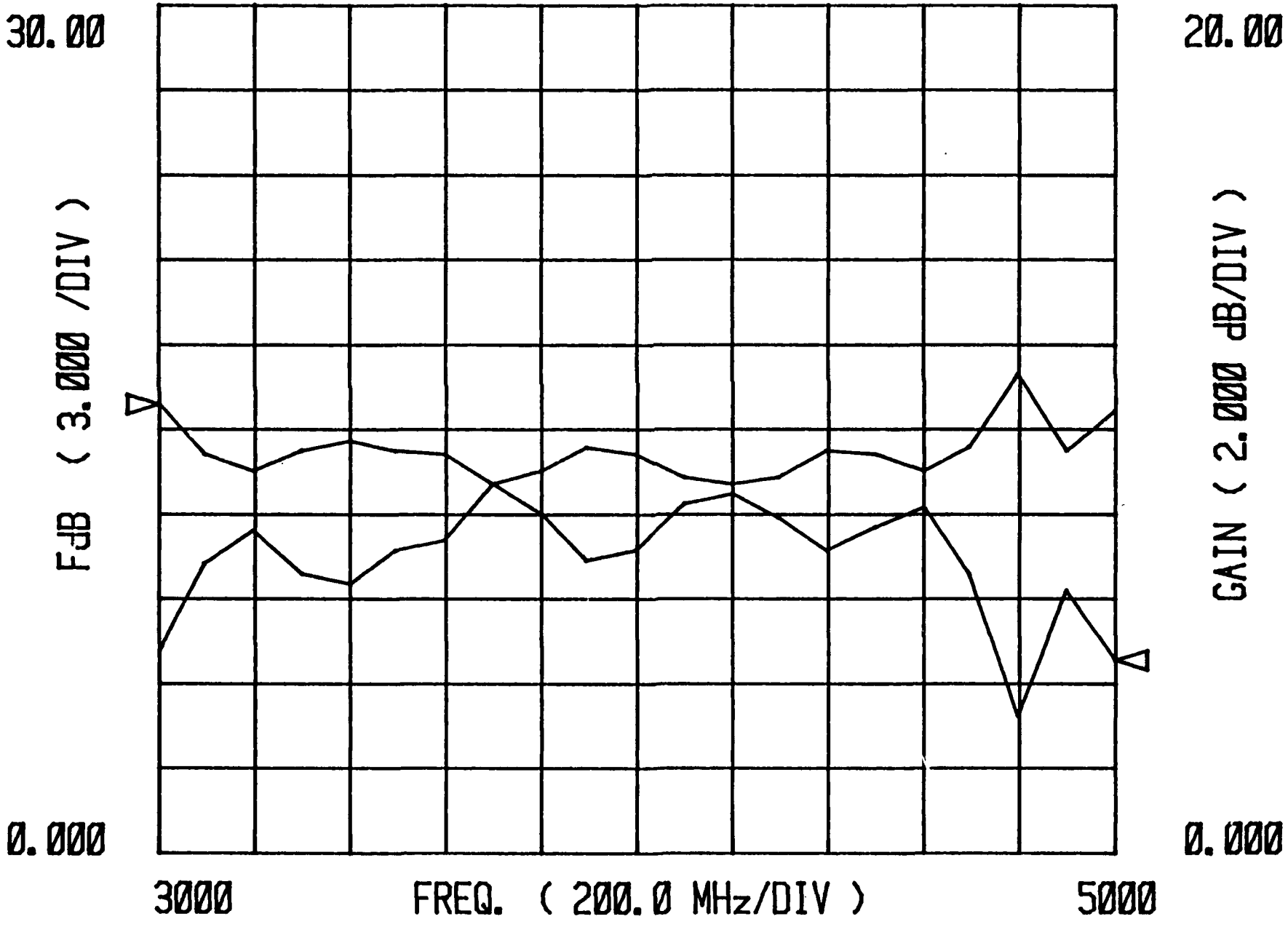
-113/71
RF 12-14 GA3
CHAN 1



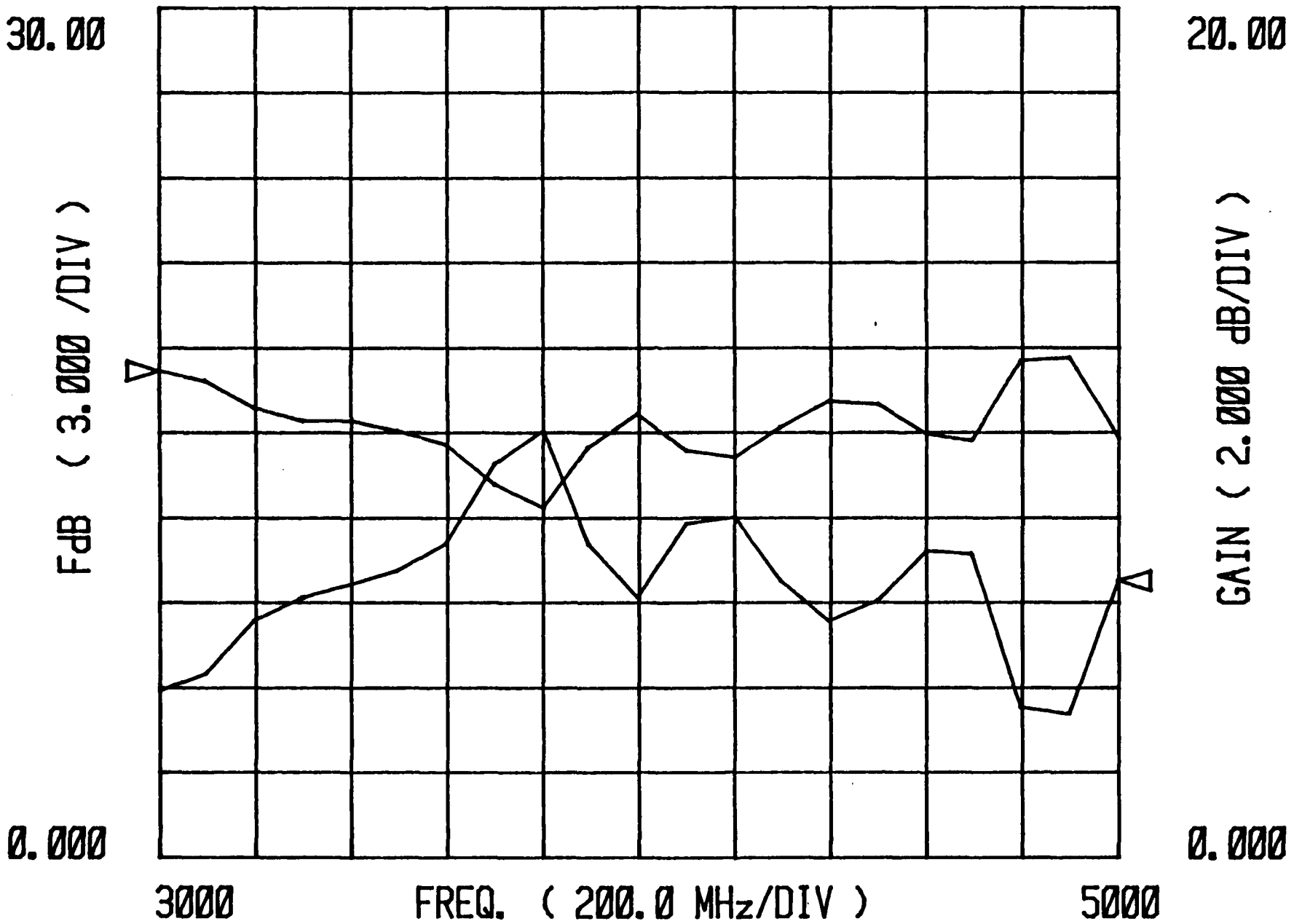
2/13/91
RF 12-14 GHz
CHAN 2



2/13/91
RF 12-146 A3
CHAN 3



4/2/71
RF 12-14 GHz
CHAN 4



4/13/71
RF 14-16 GHz
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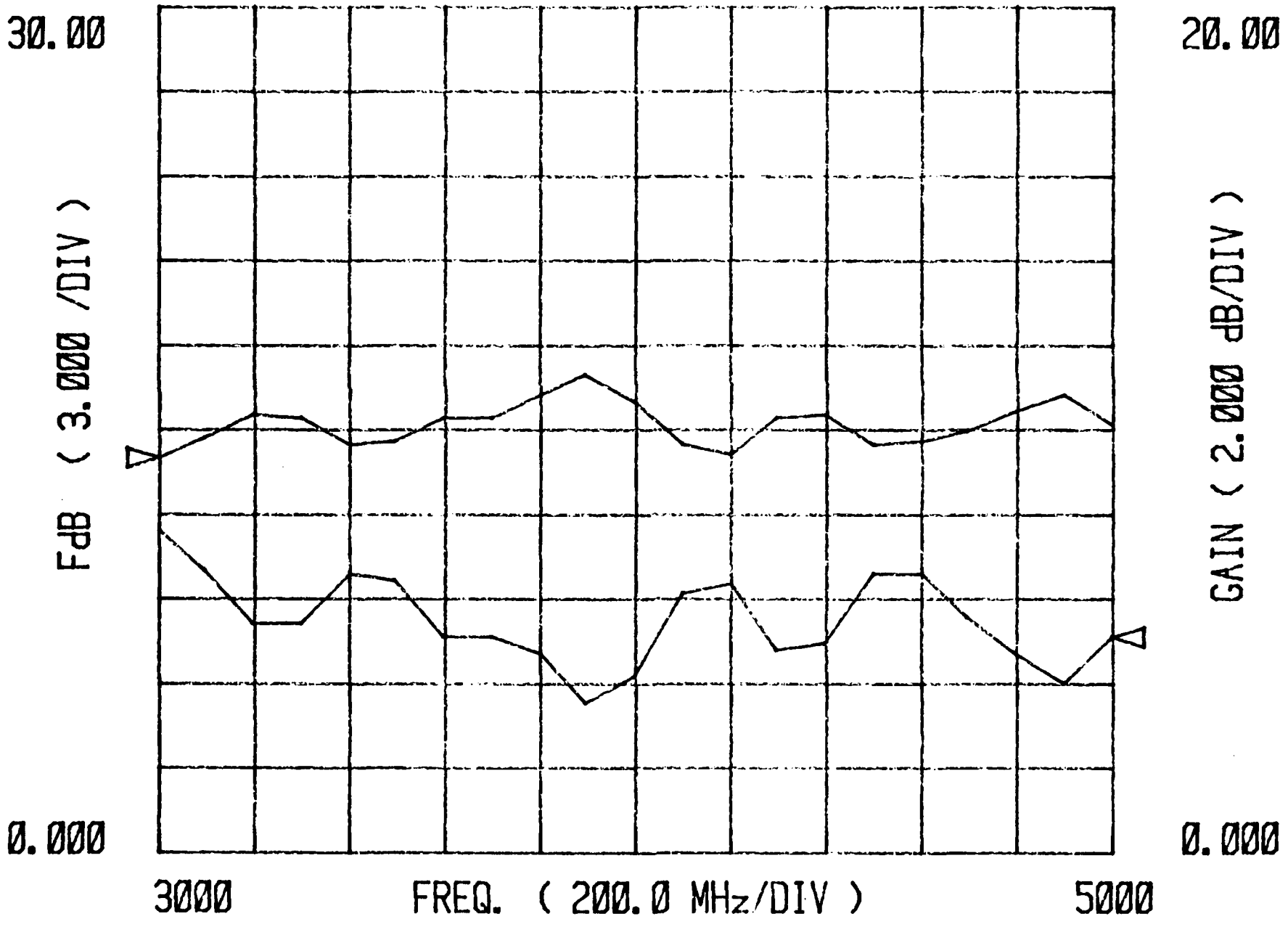
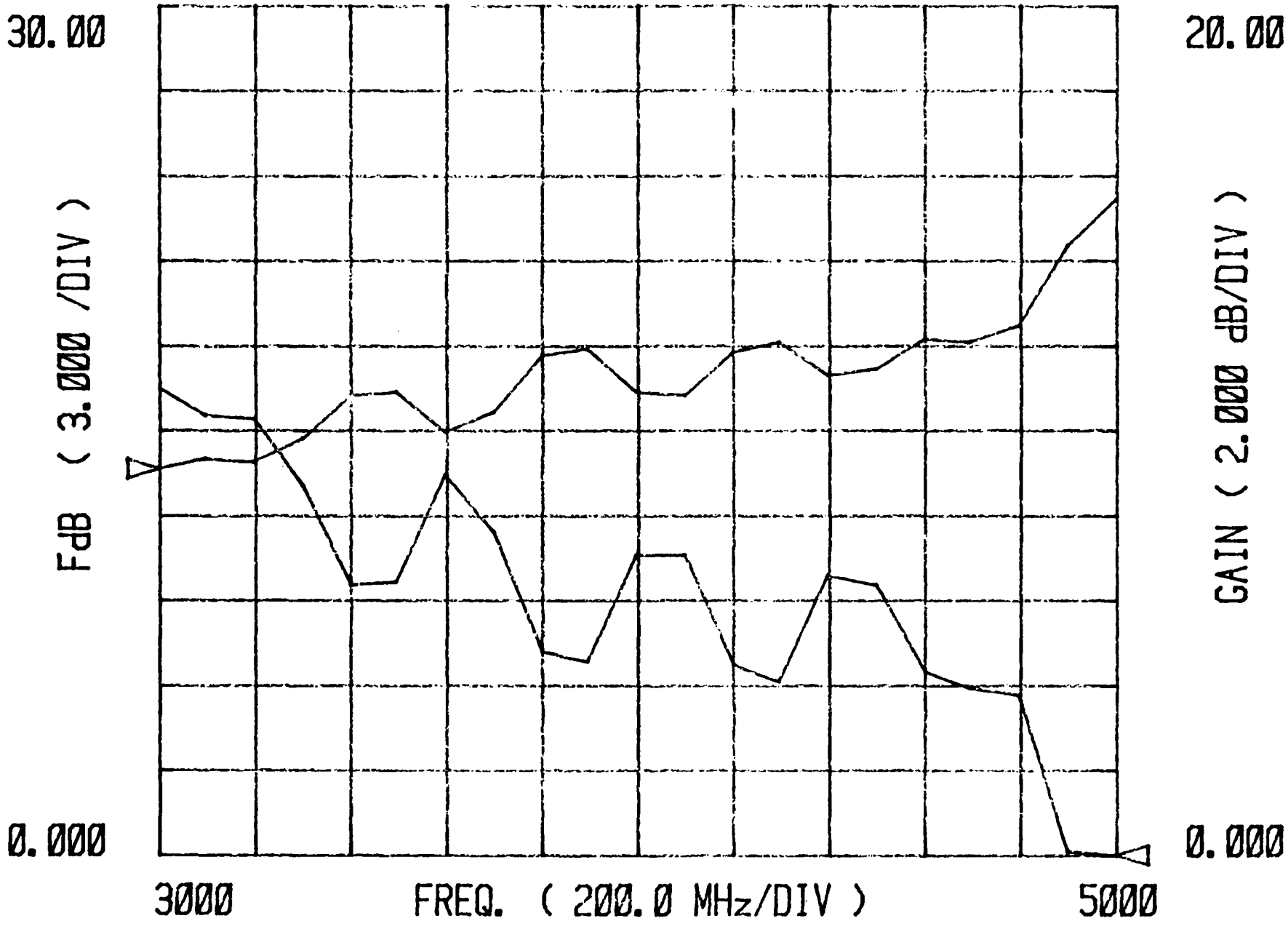
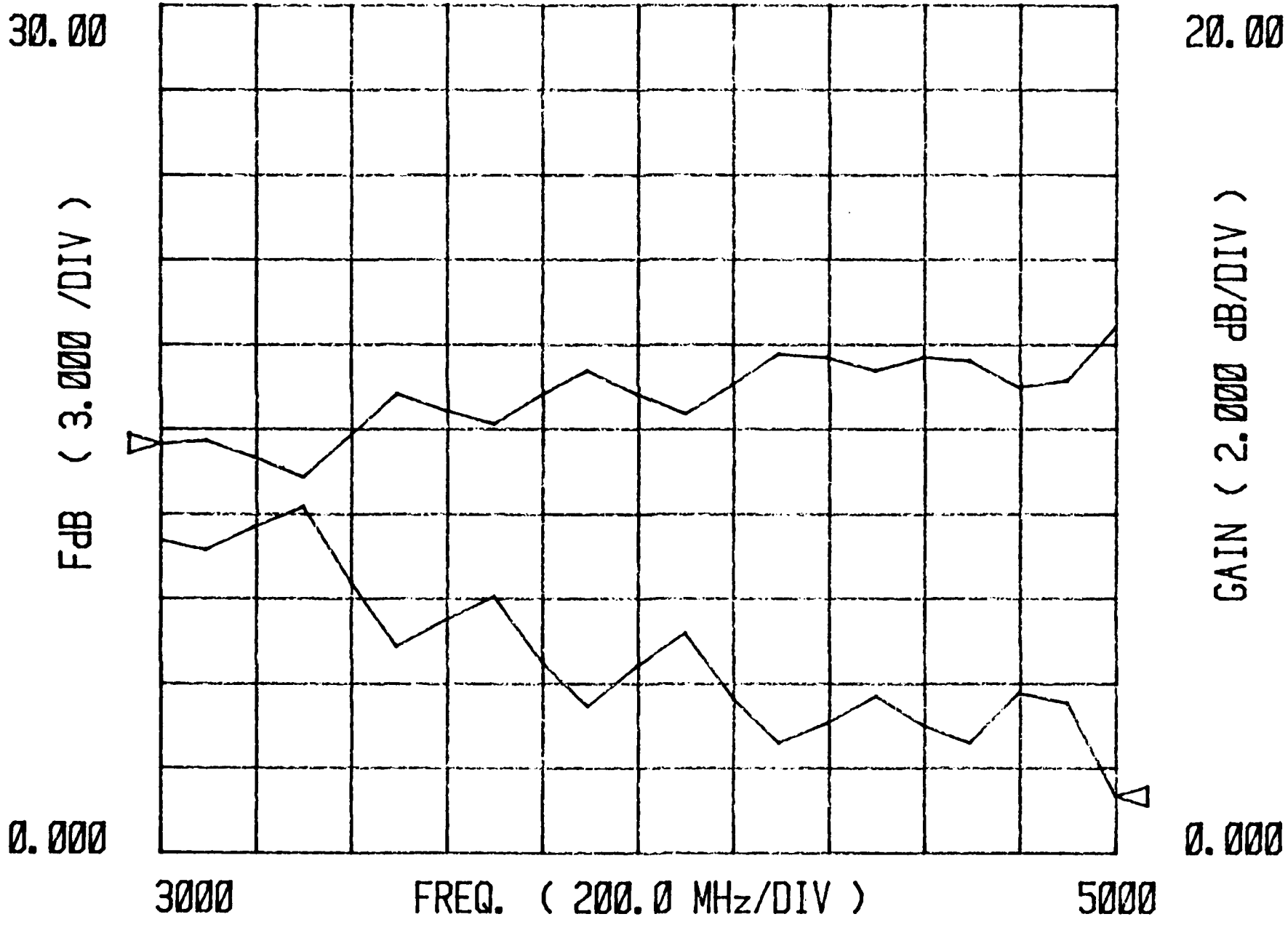


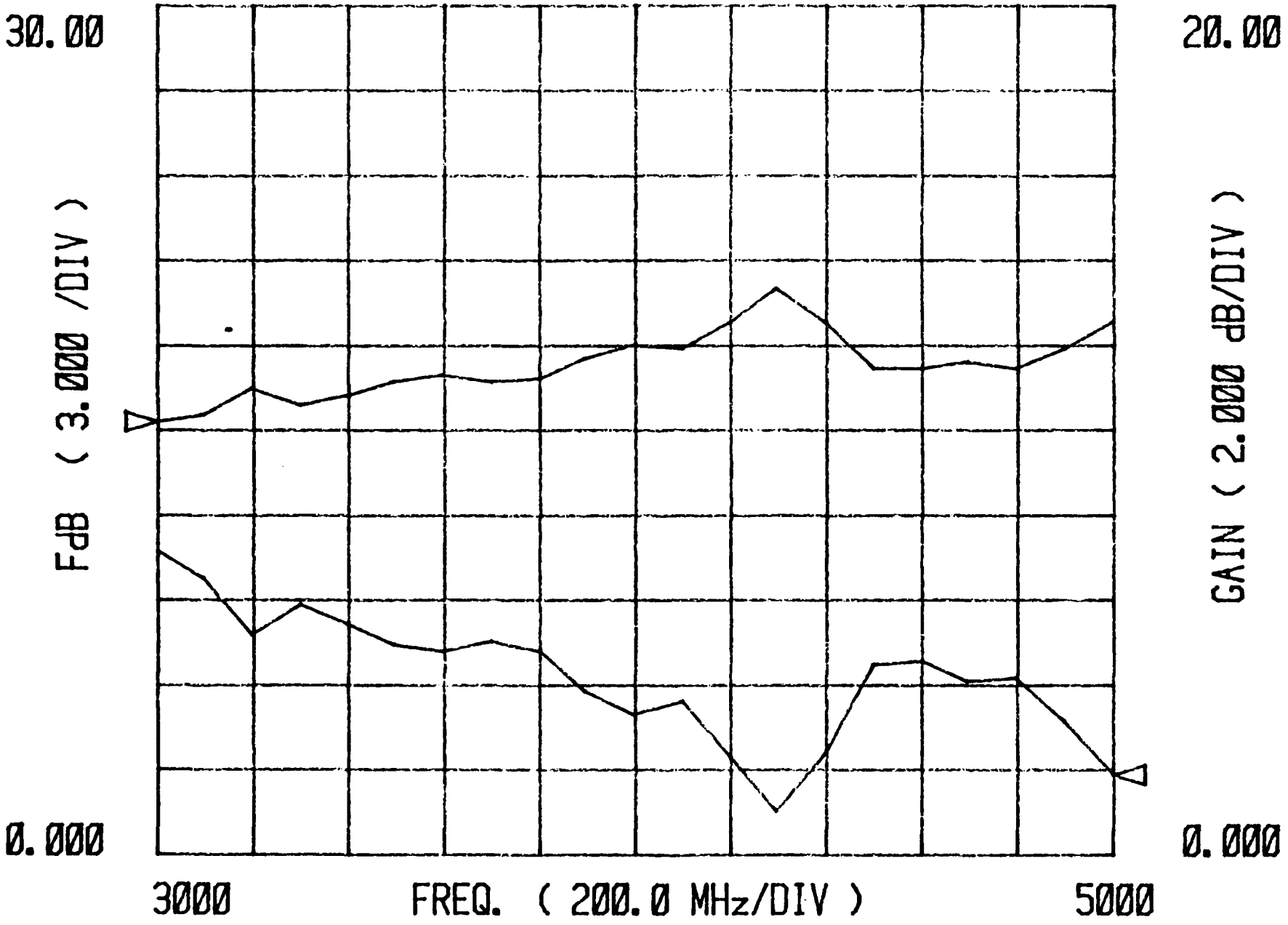
4/13/11
RF 14-16 GHz
CHAN 2



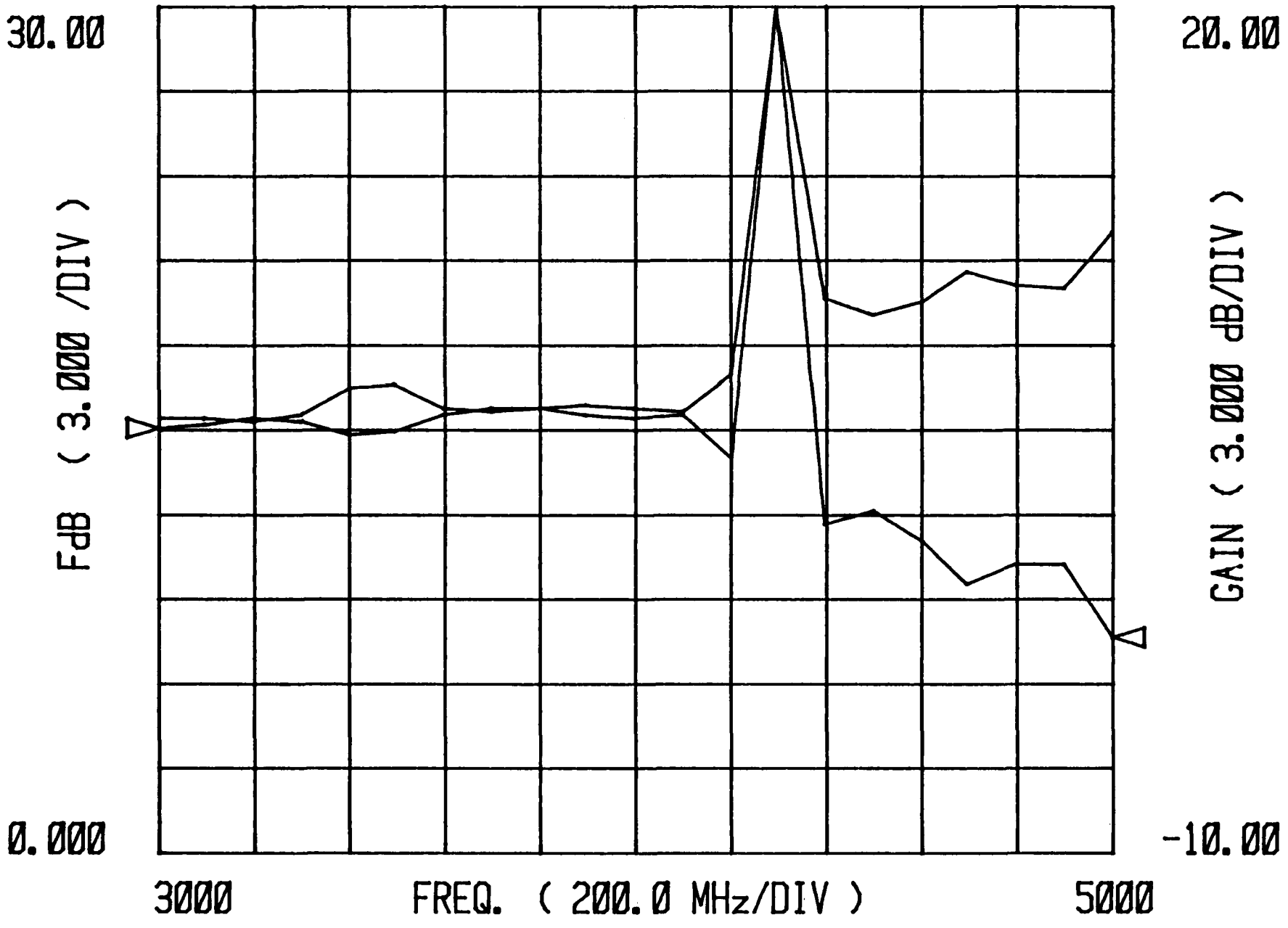
4/15/91
RF 14-16GHz
CHAN 3



4/13/71
RF 14-16 GHz
CHAN 4



1"/"
RF 16-18 GHz
CHAN 1



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RF 1678GHz
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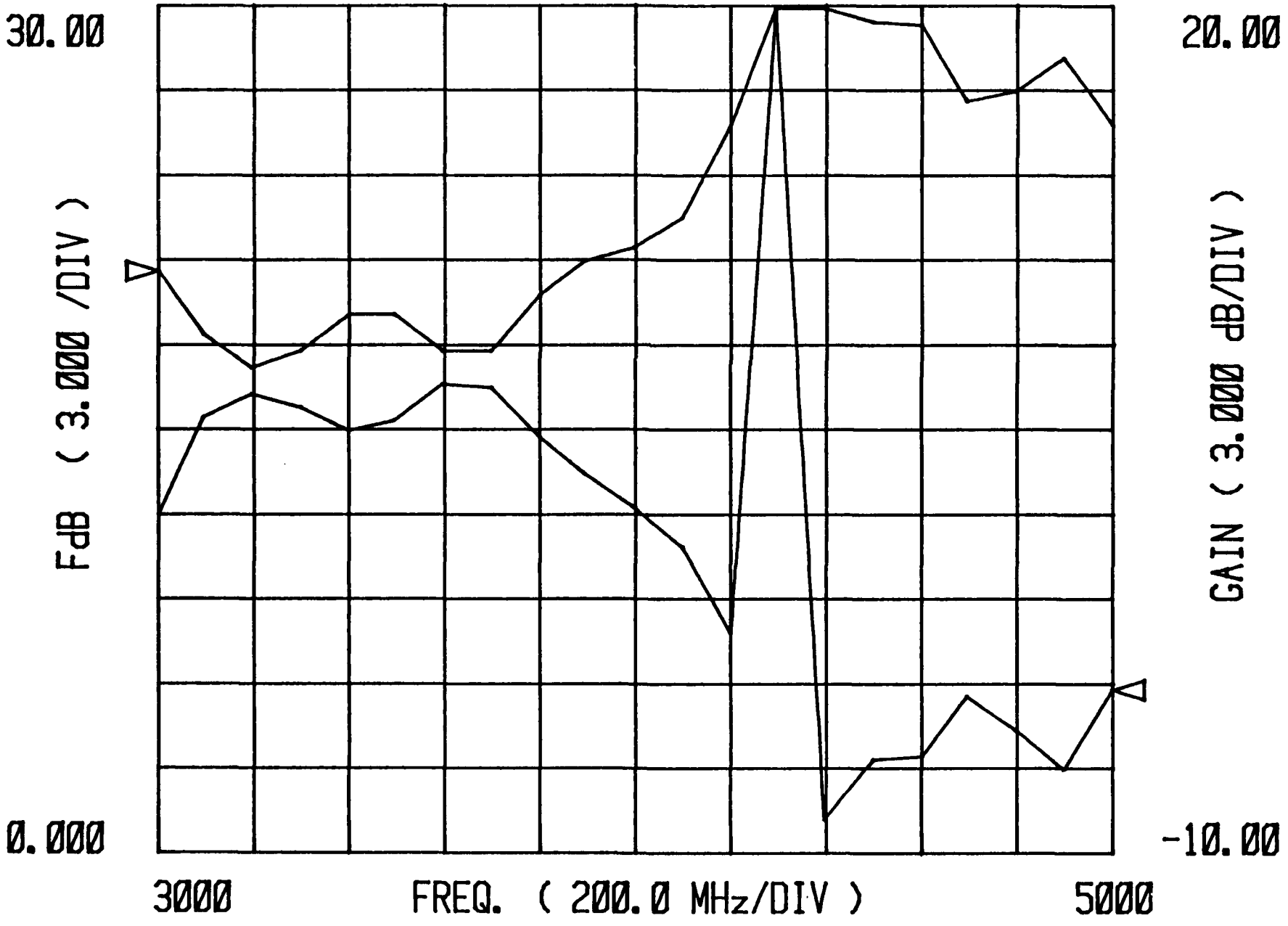

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RF 16-1864
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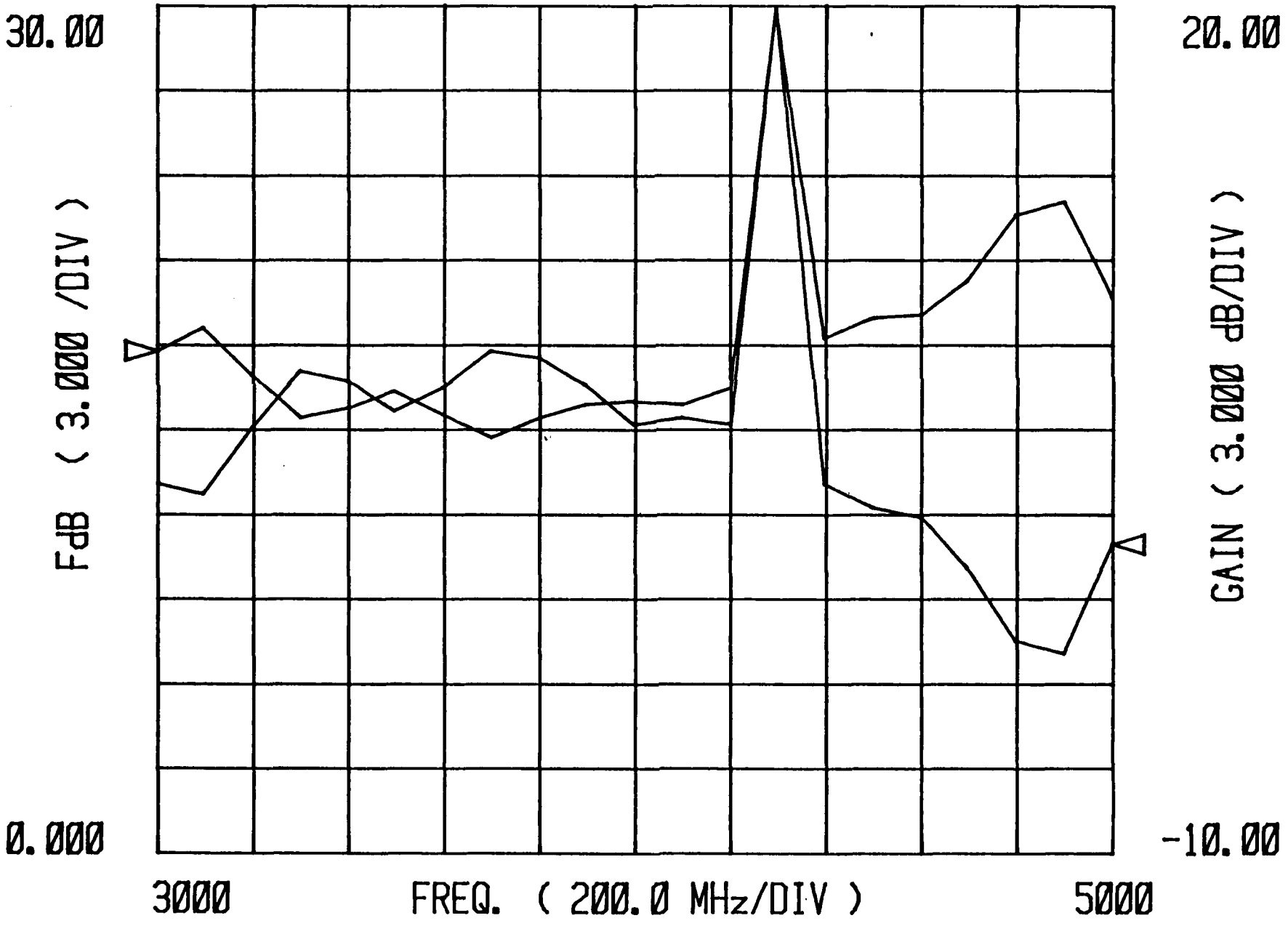
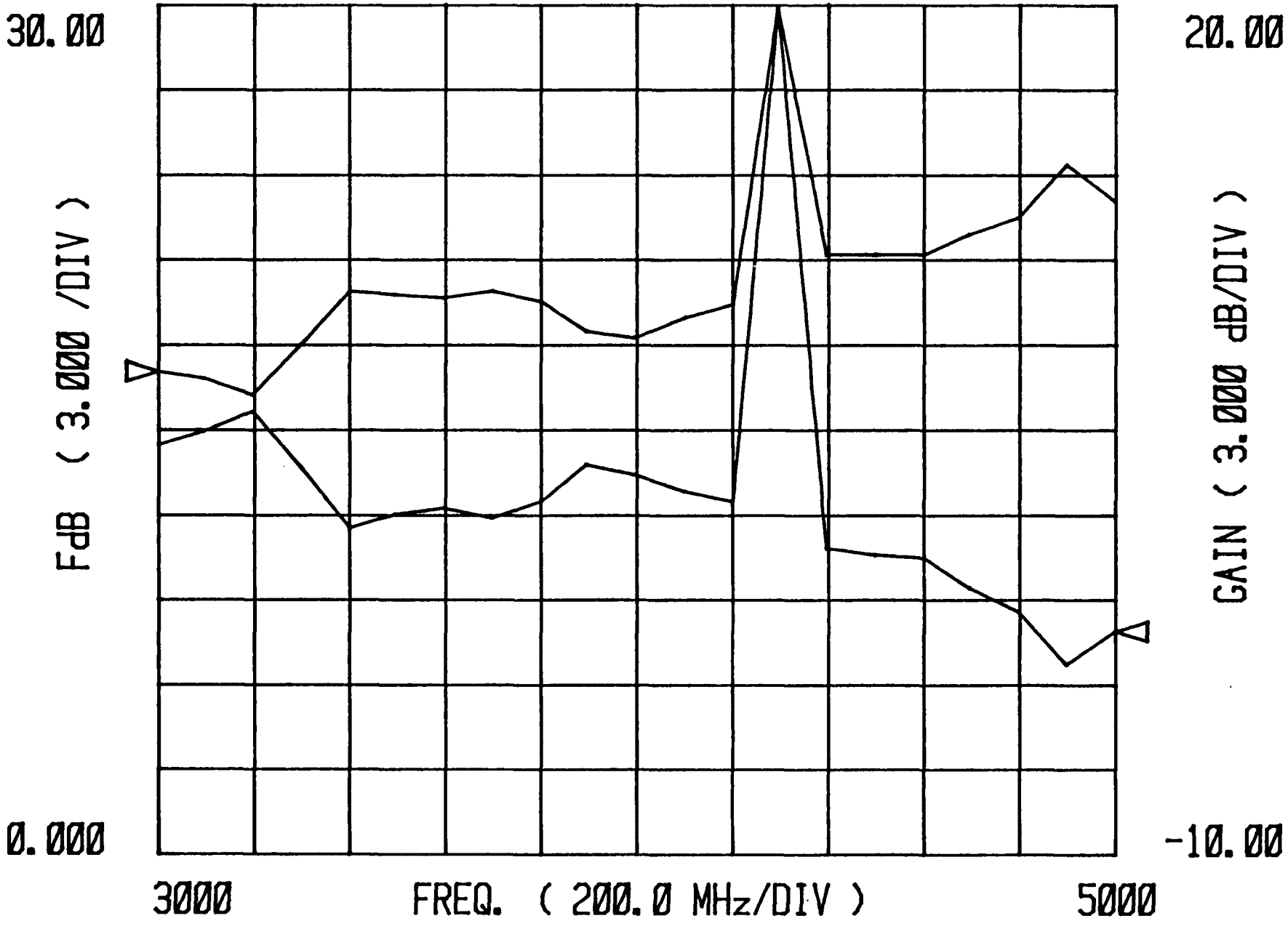


4/13/91
RF 16-18GHz
CHAN 4



Appendix B

Phase and Amplitude Tracking Data

Appendix B

Phase and Amplitude Tracking Data

The following pages are the plots of the phase- and amplitude-tracking of each subband with respect to the reference channel. The left-hand chart is the phase difference between the reference channel (channel 1) and the channel under test *versus* frequency. The right-hand chart is the amplitude plot. The hand-written symbol below the date on the right side of the sheet indicates (test channel-number, test subband-number)/(ref channel-number, ref subband-number). Following these plots are graphs that show the rms values of relative phase and amplitude for each subband. The test set-up used to measure this performance is shown in Fig. B-1.

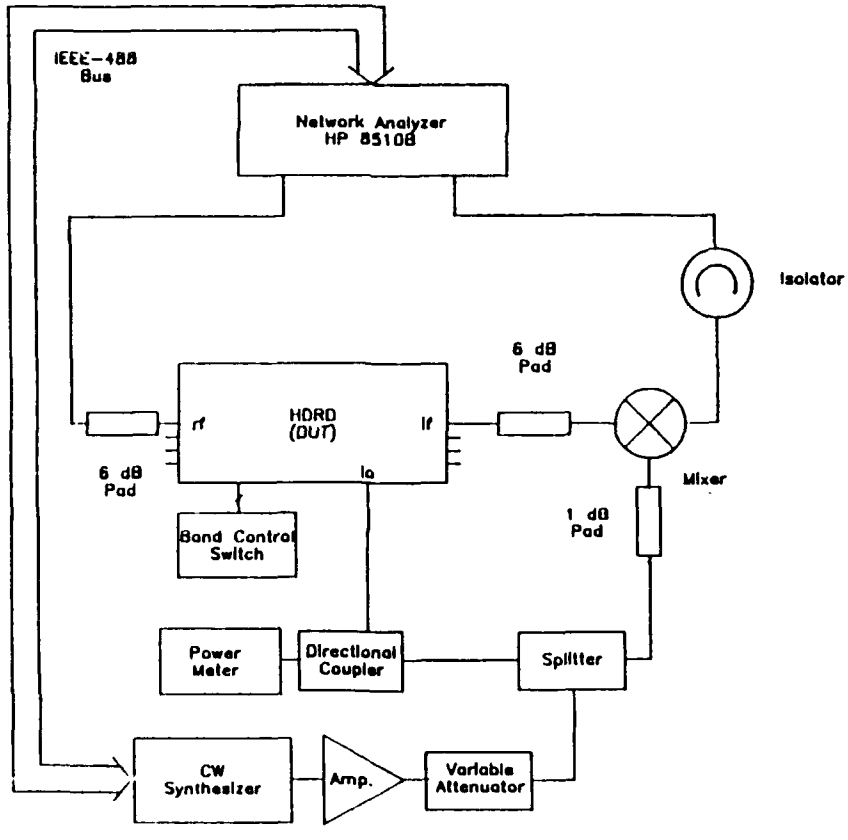
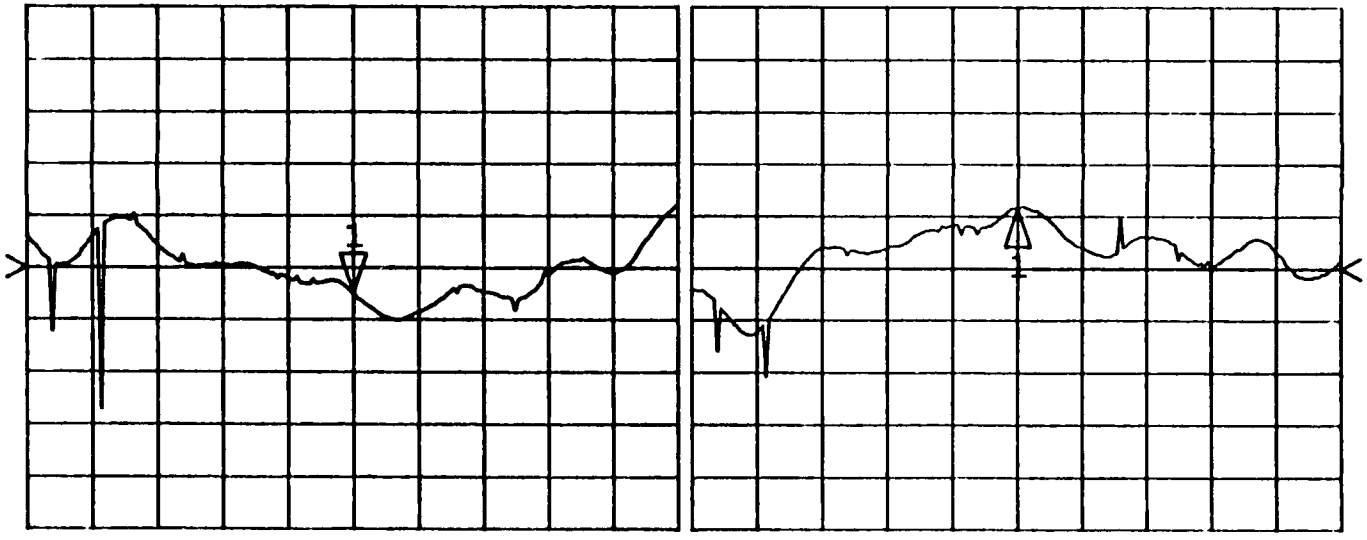


Figure B-1. HDRD tracking test set block diagram.

S_{21}/M1 ∠
REF 0.0 °
1 15.0 °/
▽ -7.1865 °
hp

S_{21}/M1 log MAG
REF 0.0 dB
△ 2.0 dB/
1 2.3486 dB



2/22/91,

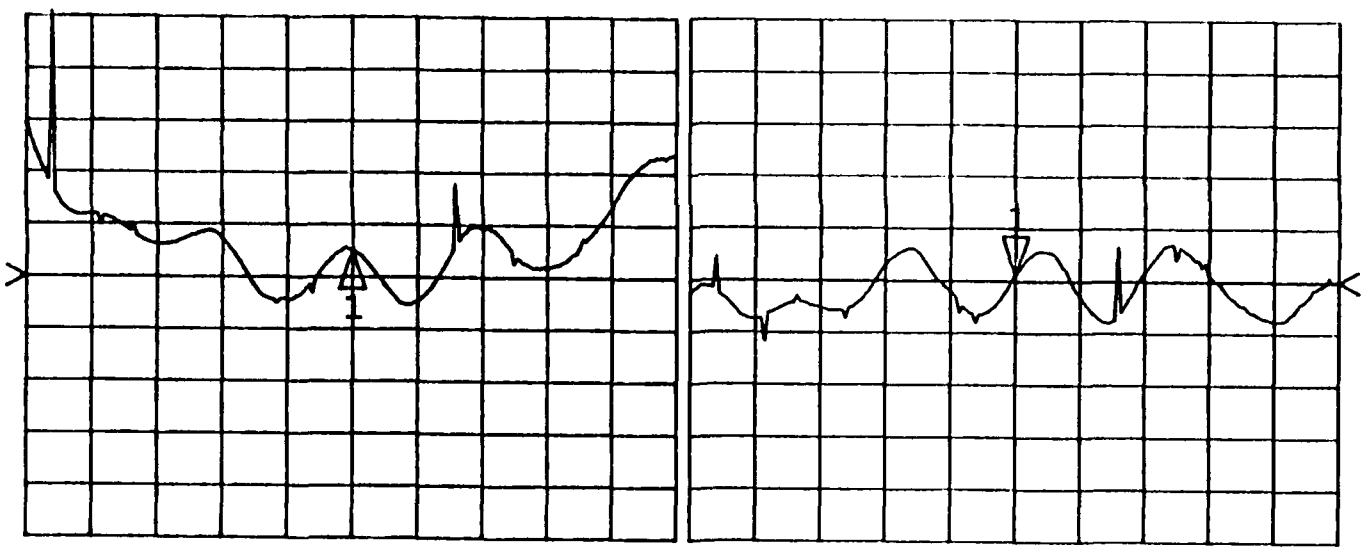
$\frac{2\ 1}{1\ 1}$ 1K

START 6.000000000 GHz
STOP 8.000000000 GHz

S21/M1 ∠
REF 0.0 °
Δ 15.0 °/
1 7.8921 °

hp

S21/M1 log MAG
REF 0.0 dB
1 2.0 dB/
▽ 0.2009 dB

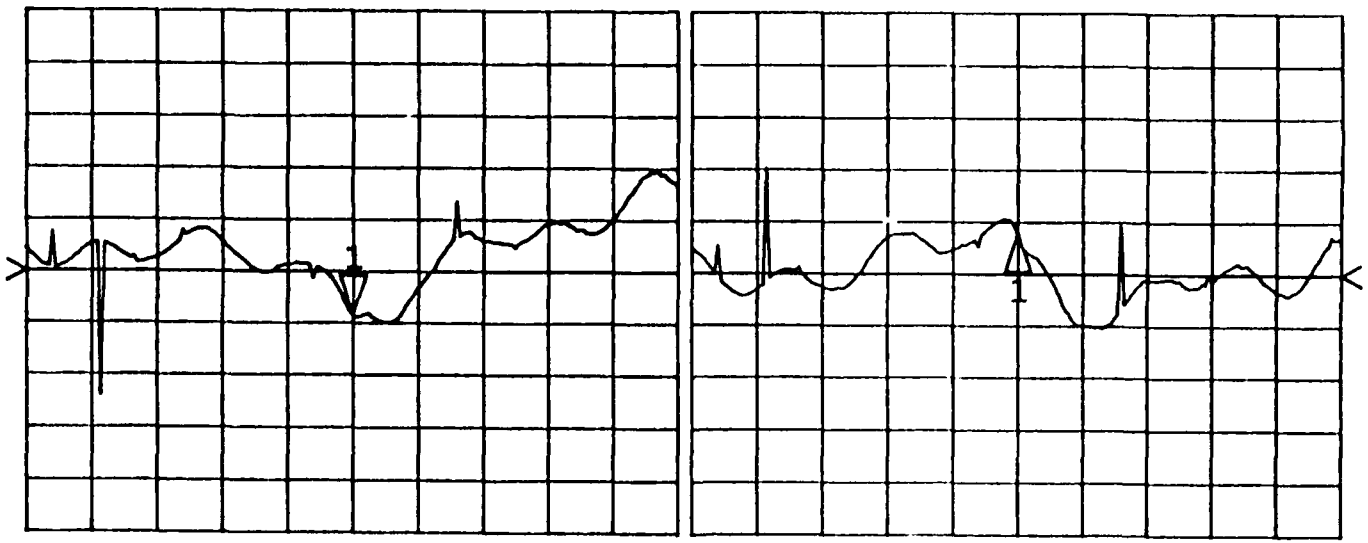


2/12/91

START 6.000000000 GHz
STOP 8.000000000 GHz

S_{21}/M1 ∠
REF 0.0 °
1 15.0 °/
▽ -12.312 °
hp

S_{21}/M1 log MAG
REF 0.0 dB
△ 2.0 dB/
1 1.6143 dB



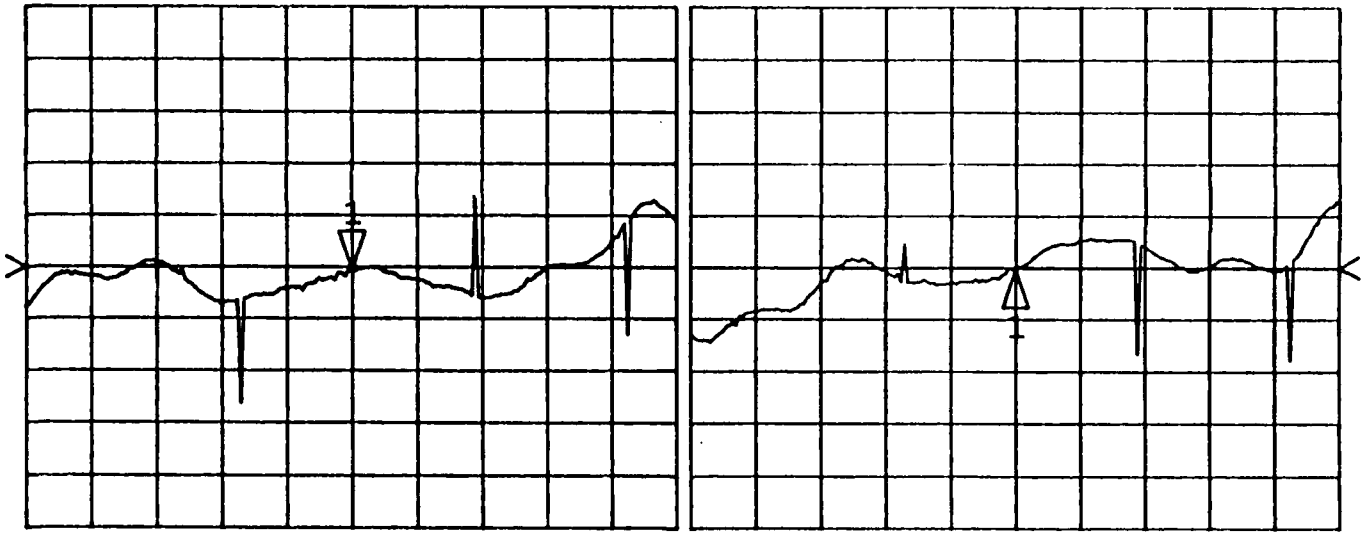
2/22/91

4 1
1 1 AK

START 6.000000000 GHz
STOP 8.000000000 GHz

S21/M2 ∠
REF 0.0 °
1 15.0 °/
-839.08 m°
hp

S21/M2 log MAG
REF 0.0 dB
2.0 dB/
1 -0.0236 dB

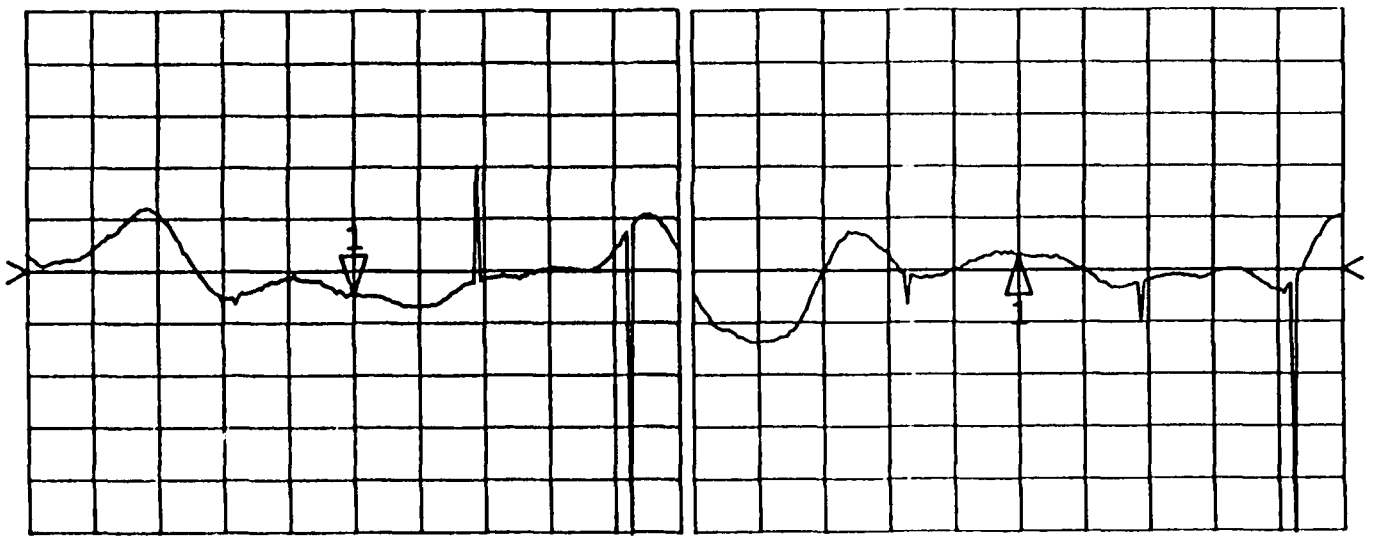


2/12/91

START 8.000000000 GHz
STOP 10.000000000 GHz

S_{21}/M2 ∠
REF 0.0 °
1 15.0 °/
▽ -6.7786 °
hp

S_{21}/M2 log MAG
REF 0.0 dB
△ 2.0 dB/
1 0.5598 dB



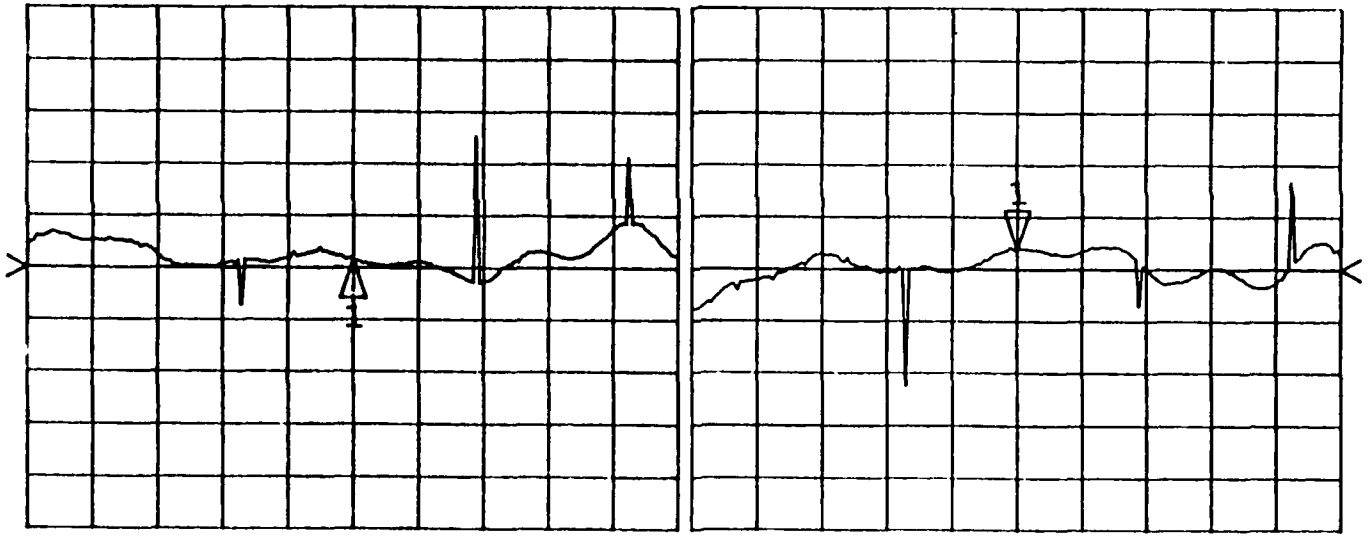
2/22/91 g

3 2
1 2 A/C

START 8.000000000 GHz
STOP 10.000000000 GHz

S_{21}/M2
REF 0.0 °
Δ 15.0 °/
1 2.6229 °
hp

S_{21}/M2 log MAG
REF 0.0 dB
1 2.0 dB/
▽ 0.7734 dB



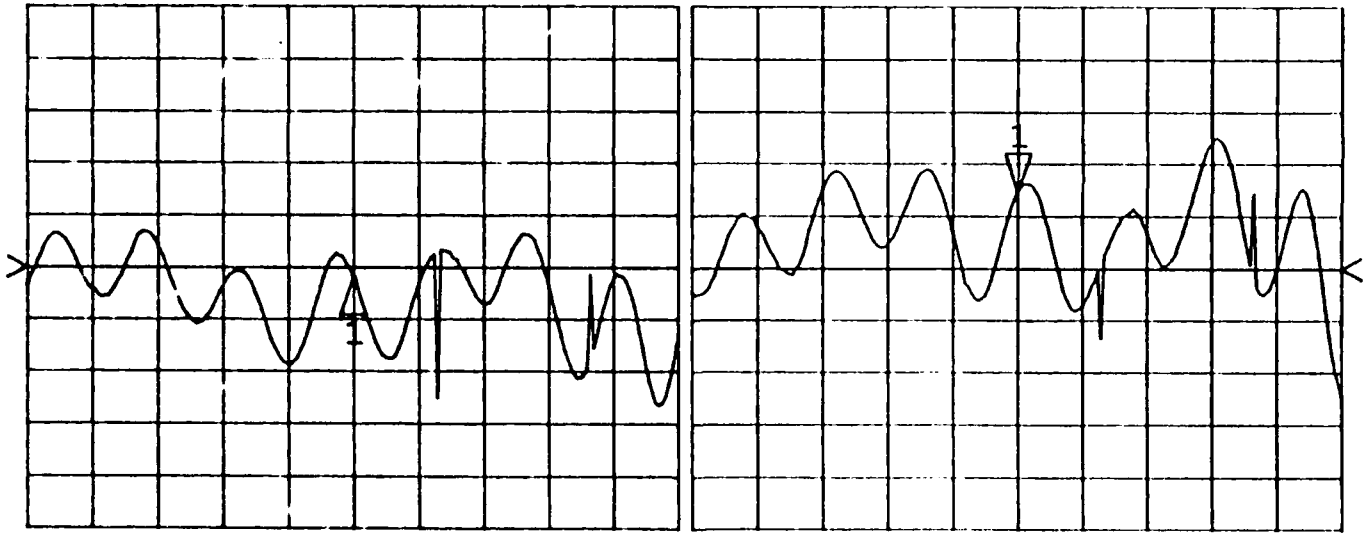
~/22/91 ?

4 L
1 L
AK

START 8.000000000 GHz
STOP 10.000000000 GHz

S_{21}/M3 ∠
REF 0.0 °
Δ 15.0 °/
1 -2.4156 °
hp

S_{21}/M3 log MAG
REF 0.0 dB
1 2.0 dB/
2.9143 dB



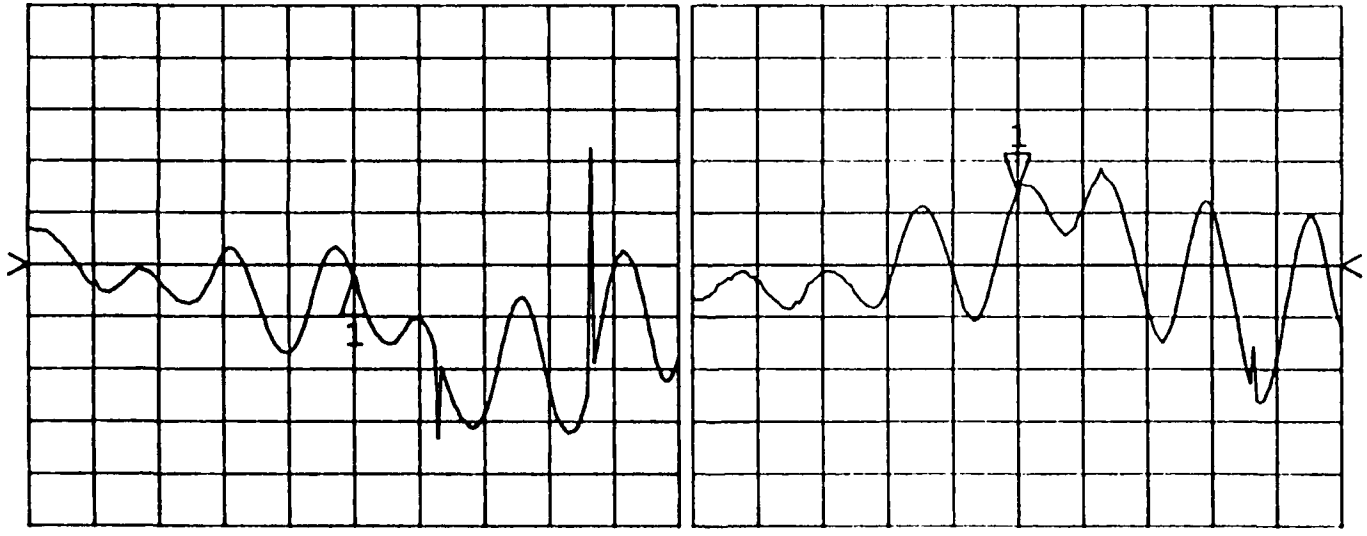
2/24/91 13

2 3
1 3 4K

START 10.000000000 GHz
STOP 12.000000000 GHz

S21/M3 ∠
REF 0.0 °
Δ 15.0 °/
1 -3.333 °
hp

S21/M3 log MAG
REF 0.0 dB
1 2.0 dB/
2.8046 dB



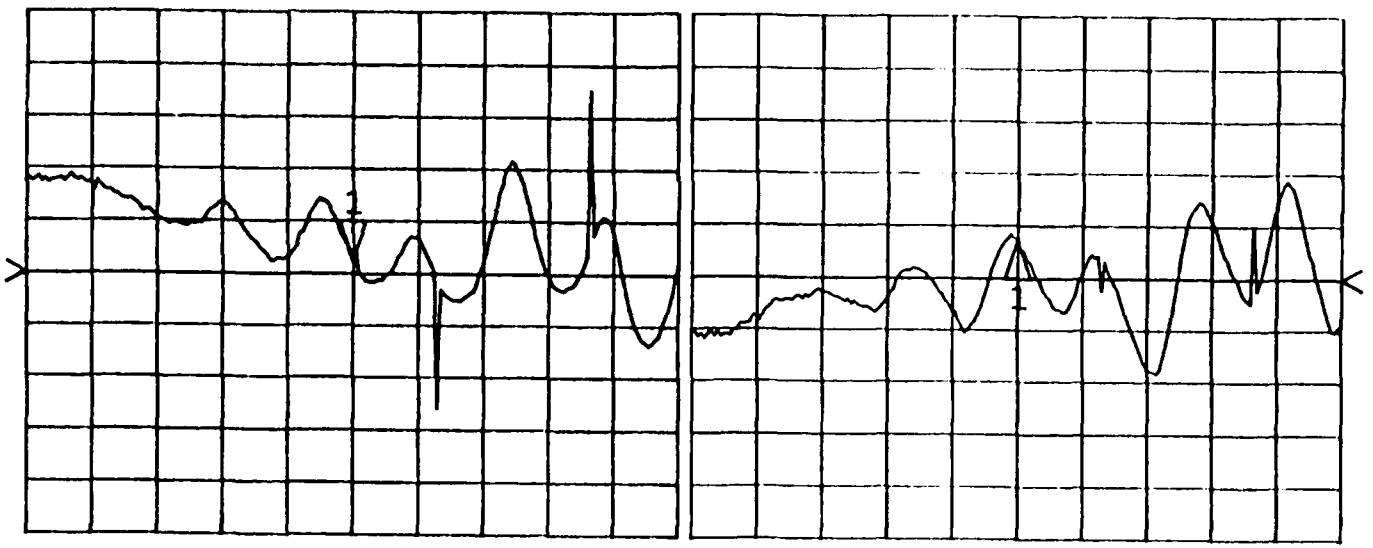
2/22/91 14

3 3
1 3 AR

START 10.000000000 GHz
STOP 12.000000000 GHz

S21/M3 ∠
REF 30.0 °
1 15.0 °/
33.898 °
hp

S21/M3 log MAG
REF -8.0 dB
Δ 2.0 dB/
1 -6.5027 dB



7/22/91 15

4 3
1 3 AK

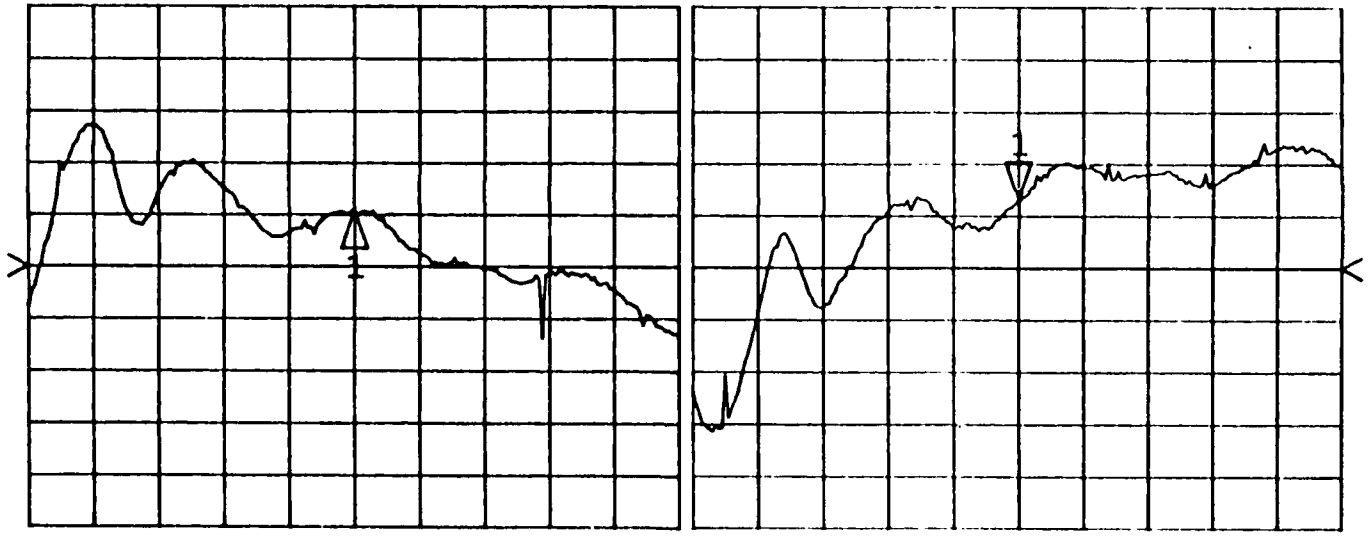
START 10.000000000 GHz
STOP 12.000000000 GHz

S21/M4 ∠
REF 0.0 °
Δ 15.0 °/
1 16.6 °

hp

*

S21/M4 log MAG
REF 0.0 dB
1 2.0 dB/
▽ 2.6077 dB



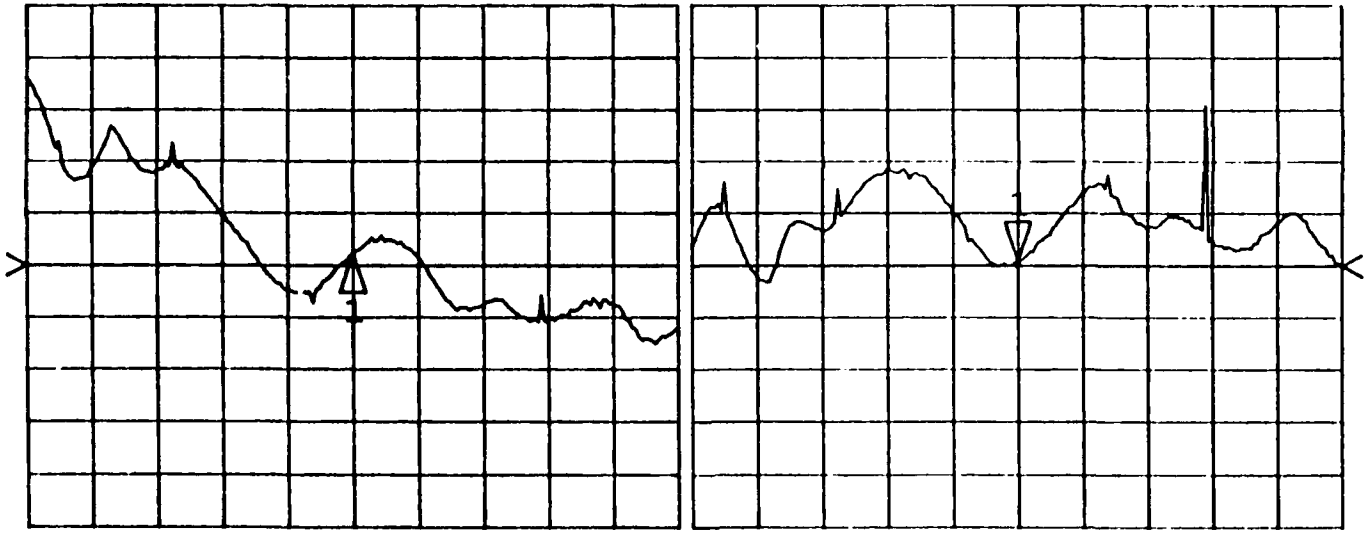
2/22/11 ,,

2 4
1 4 AK

START 12.000000000 GHz
STOP 14.000000000 GHz

S_{21}/M4 ∠
REF 0.0 °
Δ 15.0 °/
1 3.5925 °
hp

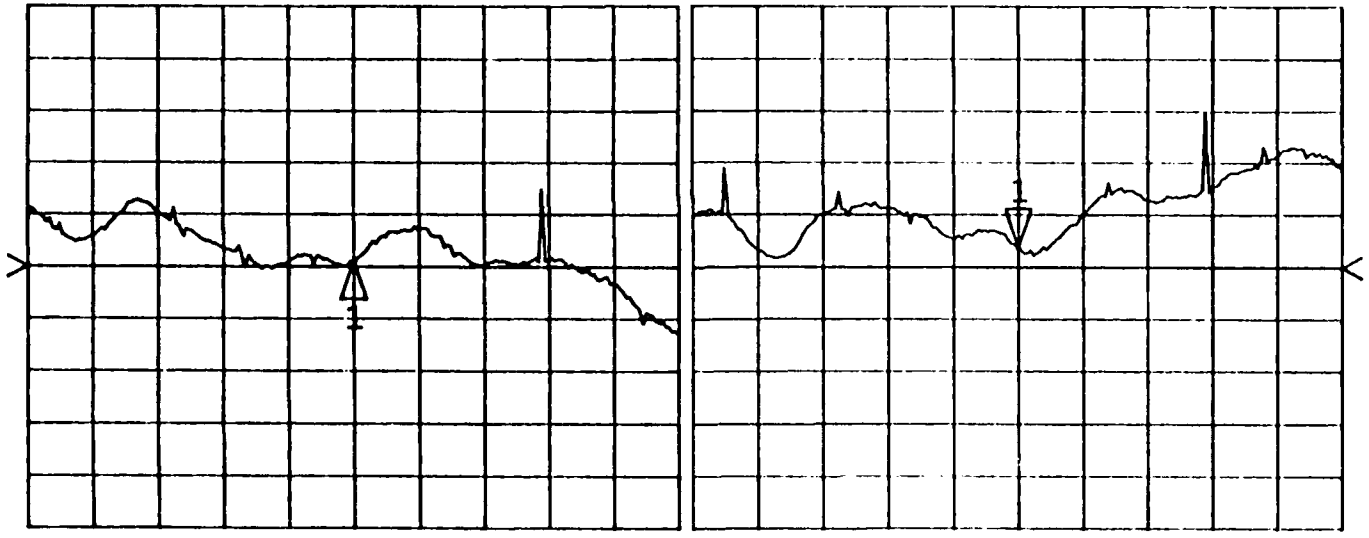
S_{21}/M4 log MAG
REF 0.0 dB
1 2.0 dB/
▽ 0.1852 dB



START 12.000000000 GHz
STOP 14.000000000 GHz

S_{21}/M4 ∠
REF 0.0 °
Δ 15.0 °/
1 2.0338 °
hp

S_{21}/M4 log MAG
REF 0.0 dB
1 2.0 dB/
0.7392 dB



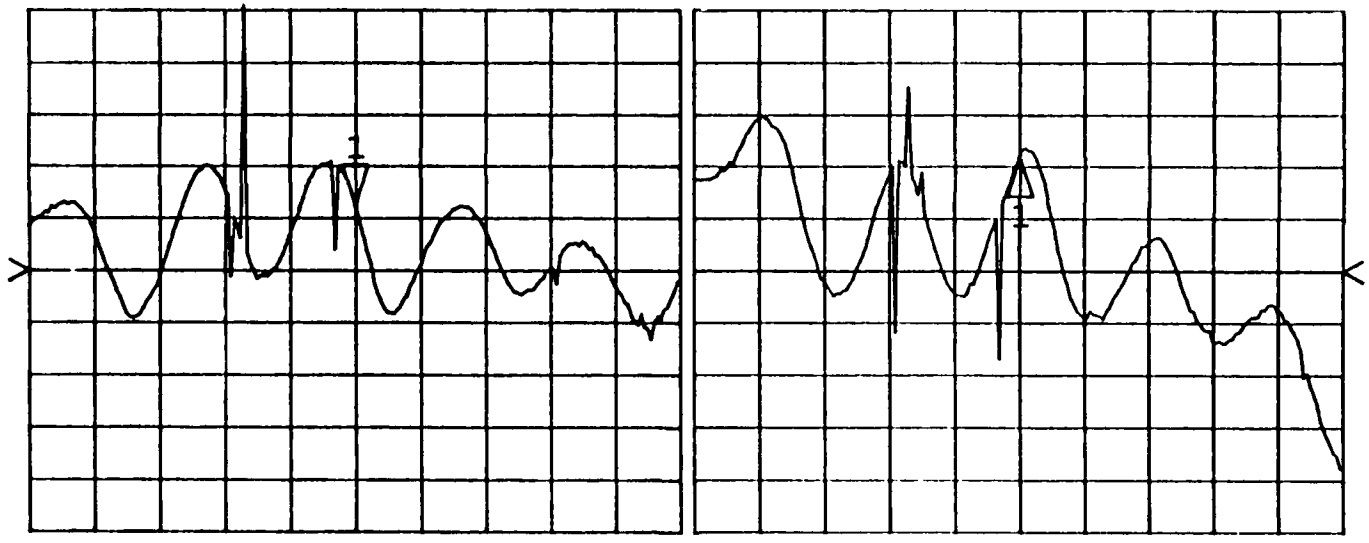
2/22/91 ,8

4 4
1 4 A/C

START 12.000000000 GHz
STOP 14.000000000 GHz

S_{21}/M5 ∠
REF 0.0 °
1 15.0 °/
19.144 °
hp

S_{21}/M5 log MAG
REF 0.0 dB
Δ 2.0 dB/
1 4.3721 dB



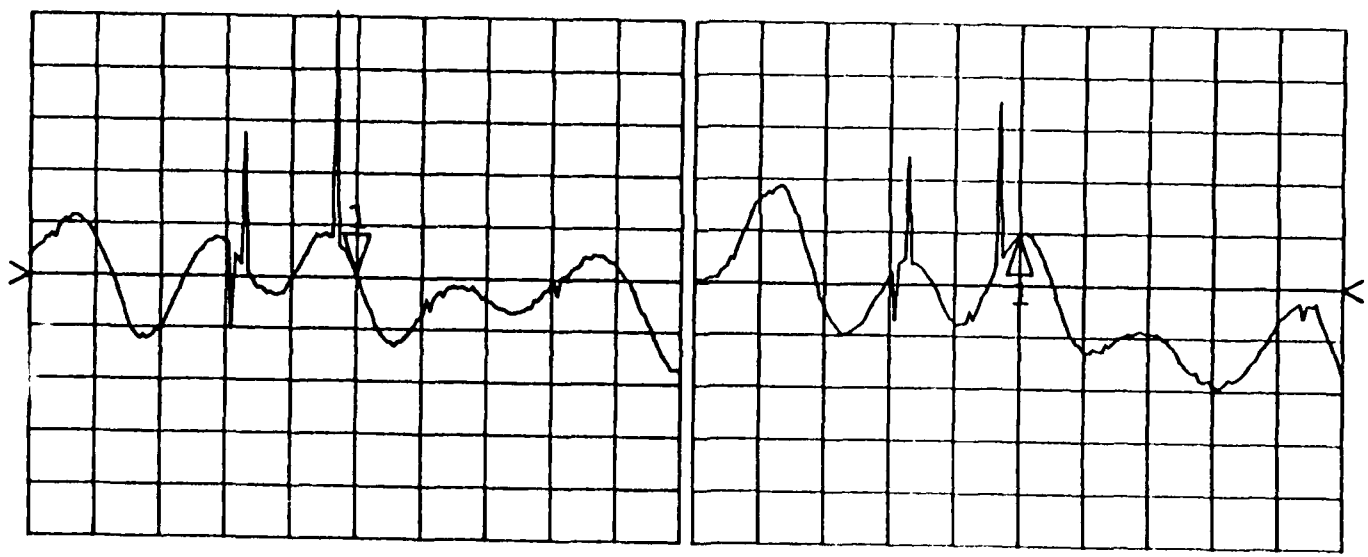
2/22/91 4

2 5
1 5 1K

START 14.000000000 GHz
STOP 16.000000000 GHz

S21/M5 ∠
REF 0.0 °
1 15.0 °/
▽ 1.2772 °
hp

S21/M5 log MAG
REF 0.0 dB
△ 2.0 dB/
1 1.9438 dB



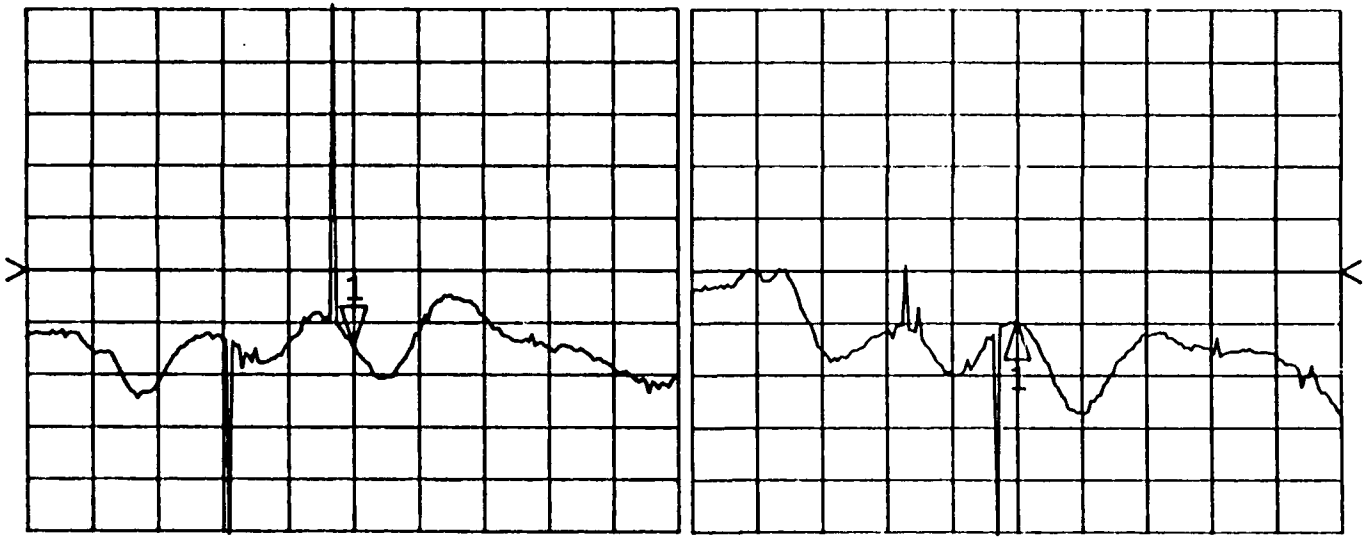
2/22/91 5

3 5
1 5 AK

START 14.000000000 GHz
STOP 16.000000000 GHz

S21/M5 ∠
REF 0.0 °
1 15.0 °/
▽ -21.513 °
hp

S21/M5 log MAG
REF 0.0 dB
△ 2.0 dB/
1 -1.8854 dB



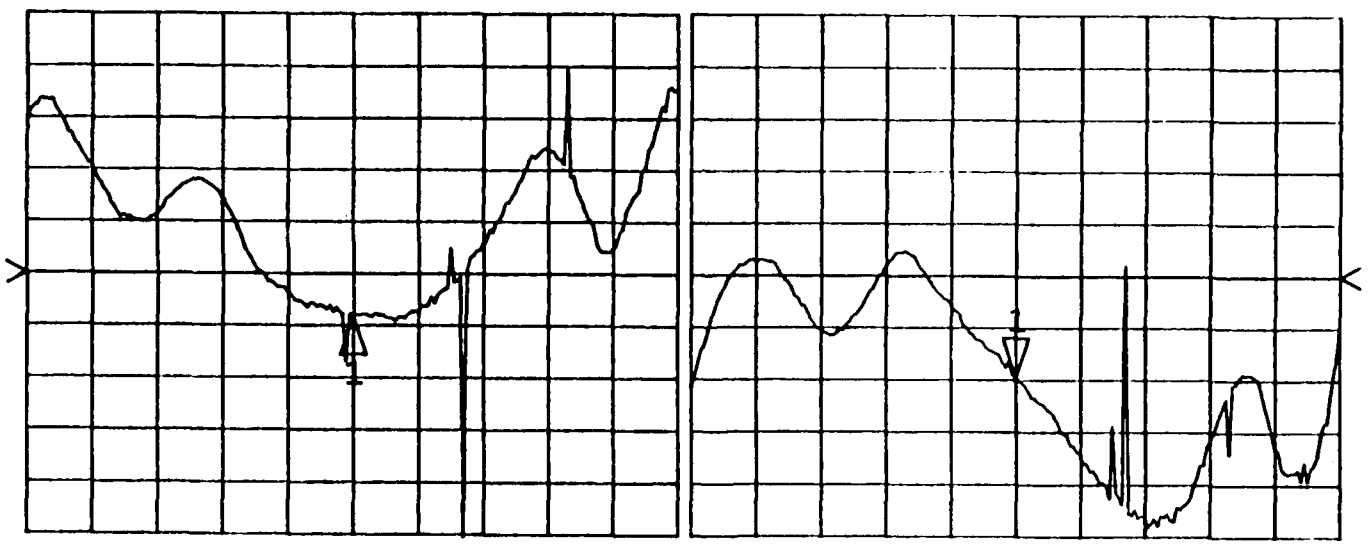
2/22/91

4 5
1 5

START 14.000000000 GHz
STOP 16.000000000 GHz

S21/M6 ∠
REF 0.0 °
Δ 15.0 °/
1 -12.084 °
hp

S21/M6 log MAG
REF 0.0 dB
1 2.0 dB/
-3.8732 dB



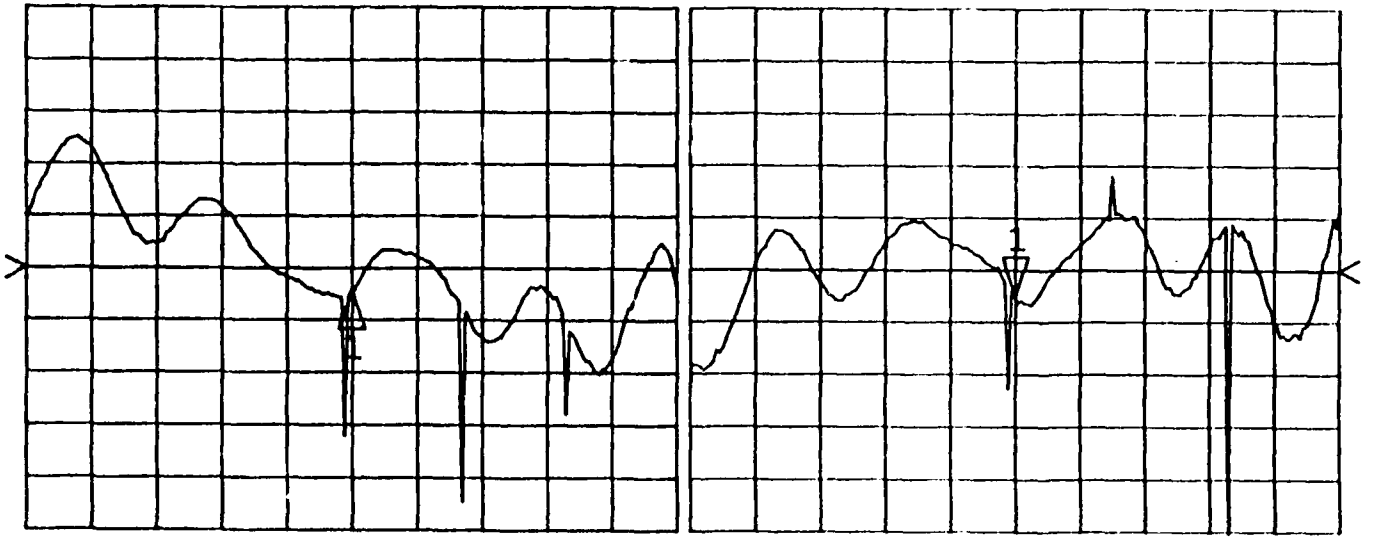
2/22/91 10

26/16 4K

START 16.000000000 GHz
STOP 18.000000000 GHz

S21/M6 ∠
REF 0.0 °
Δ 15.0 °/
1 -6.2637 °
hp

S21/M6 log MAG
REF 0.0 dB
1 2.0 dB/
▽ -0.9761 dB



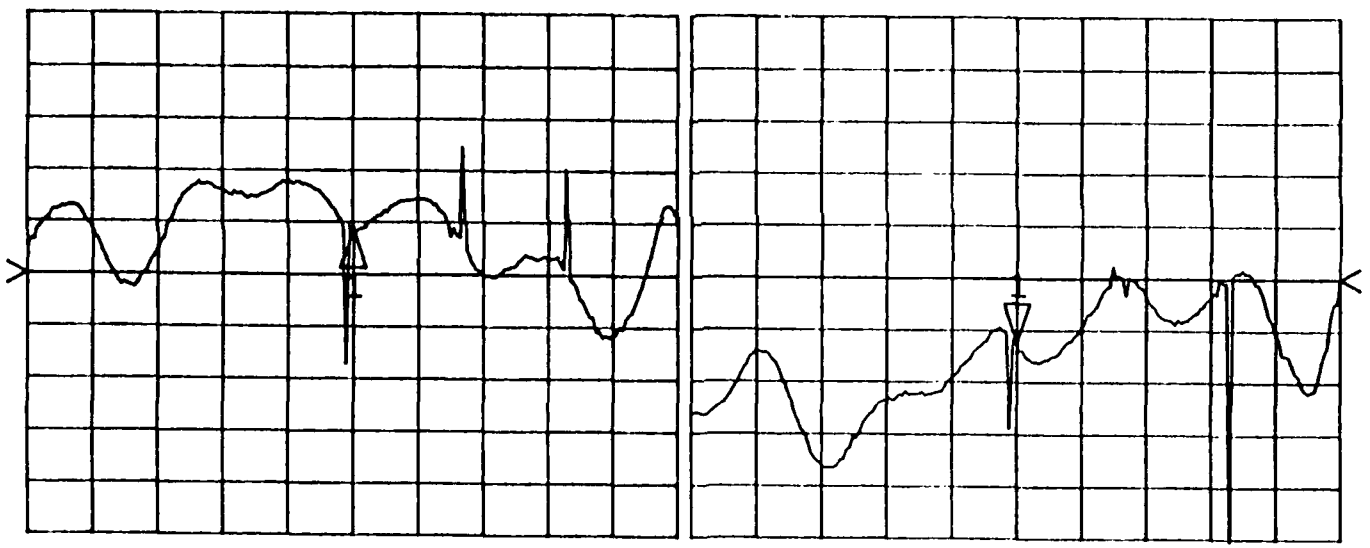
START 16.000000000 GHz
STOP 18.000000000 GHz

2/22/91 "

3 6
1 6 4K

S21/M6 ∠
REF 0.0 °
Δ 15.0 °/
1 13.226 °
hp
*

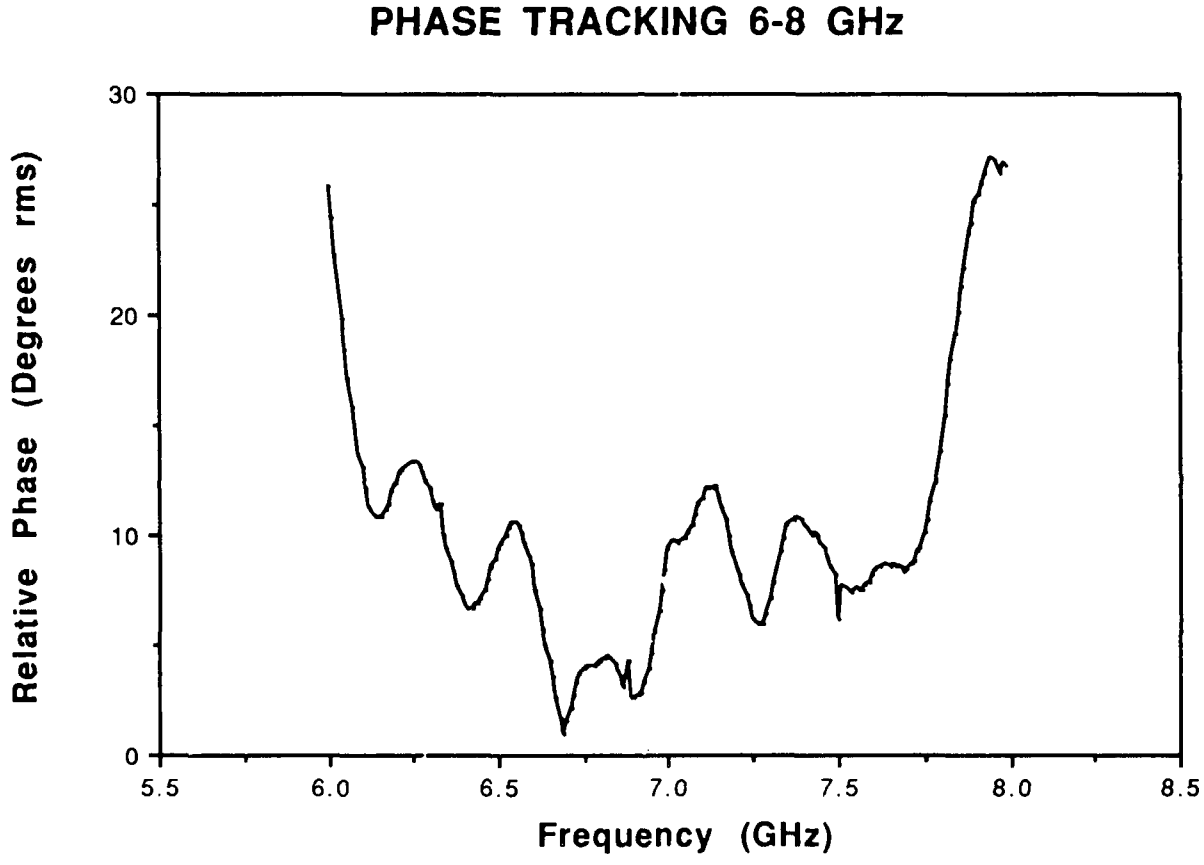
S21/M6 log MAG
REF 0.0 dB
1 2.0 dB/
▽ -2.4564 dB

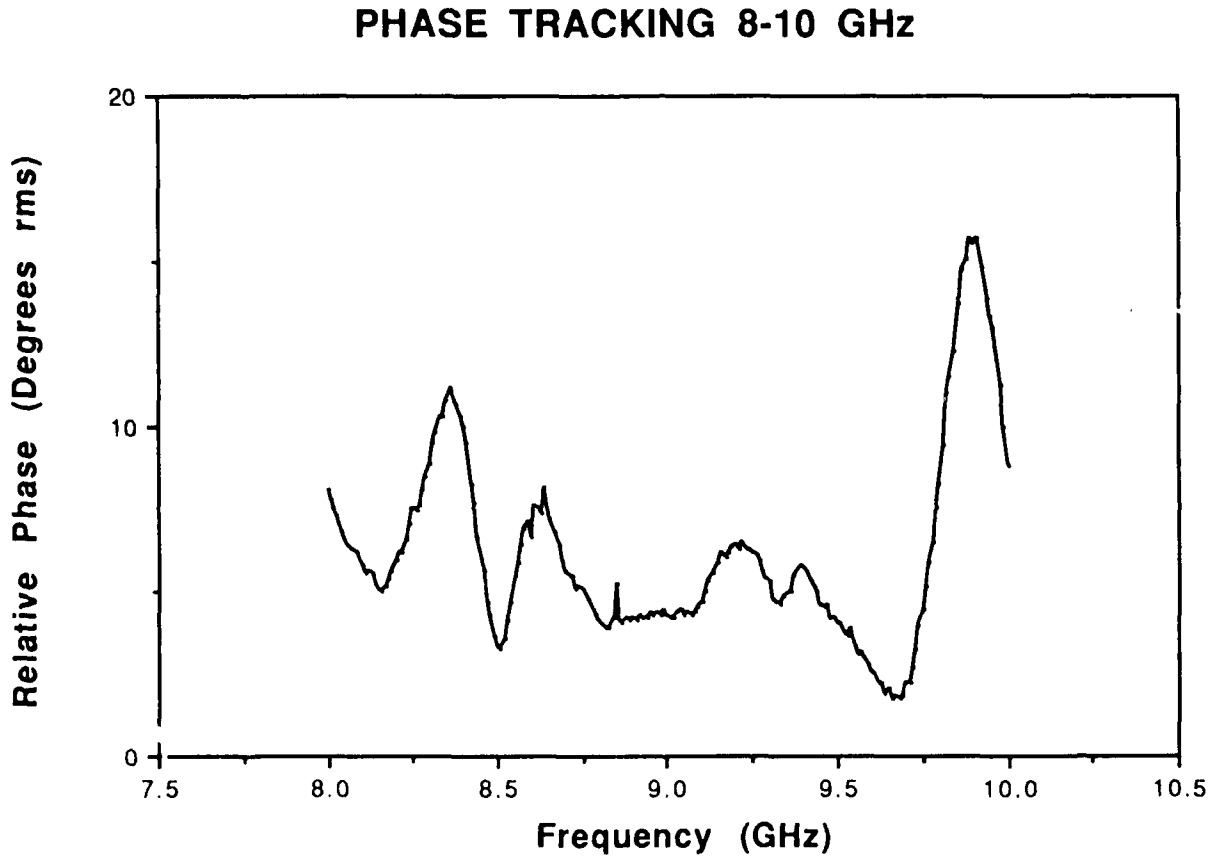


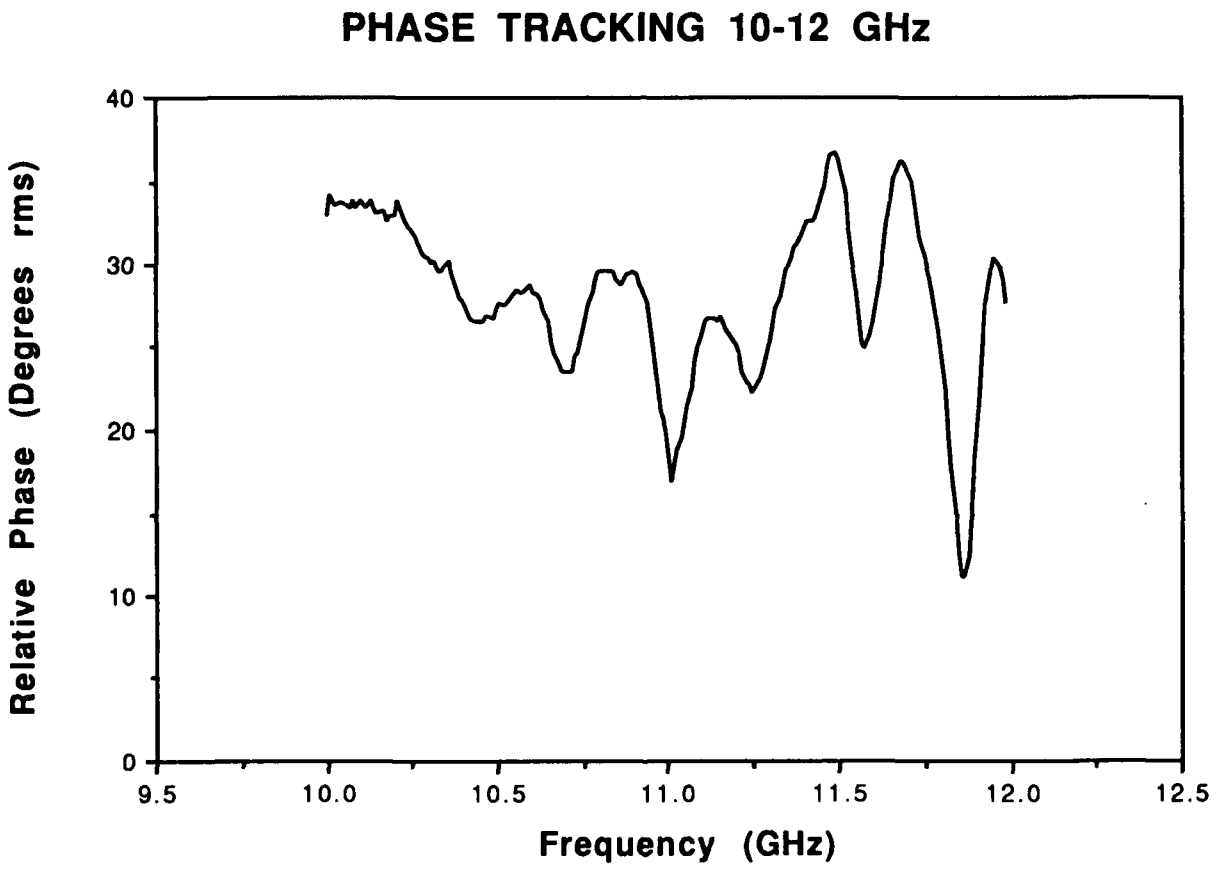
2/22/91 IL

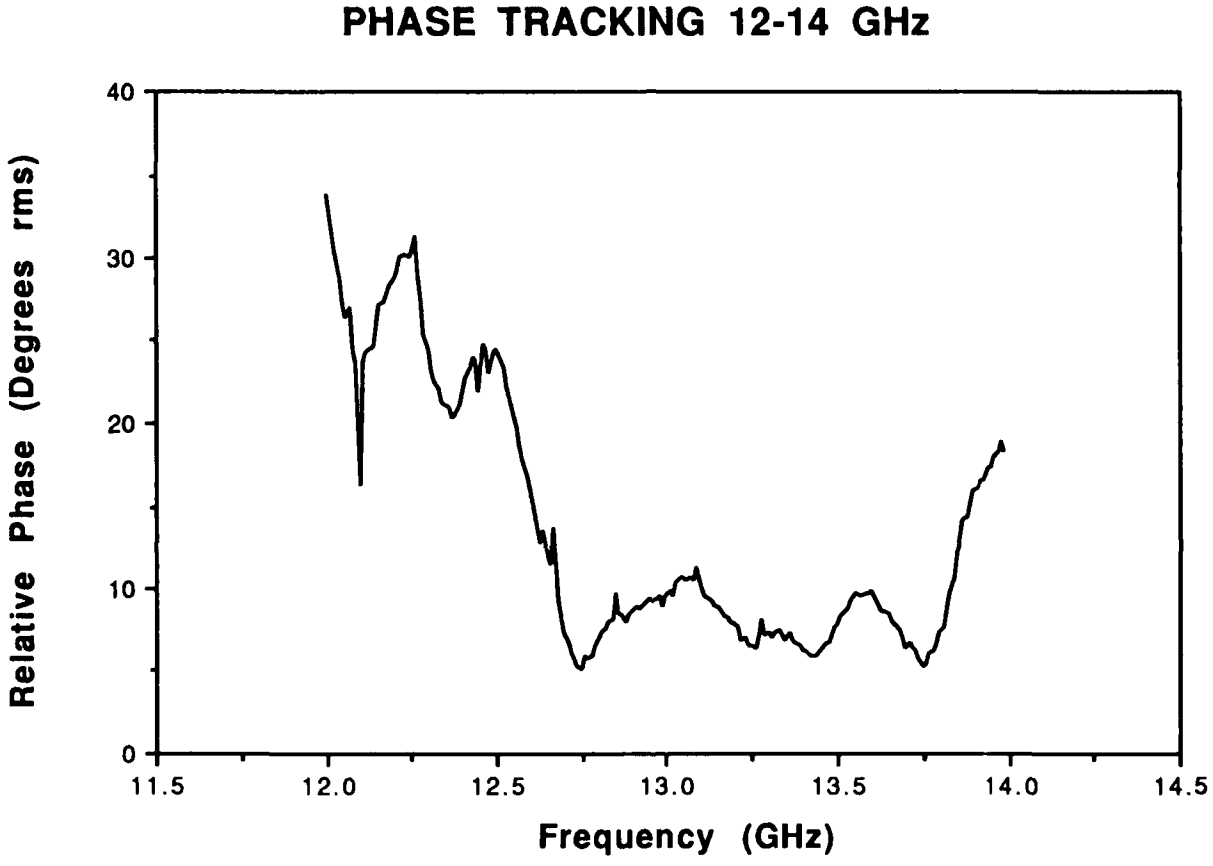
4 6
1 6 1K

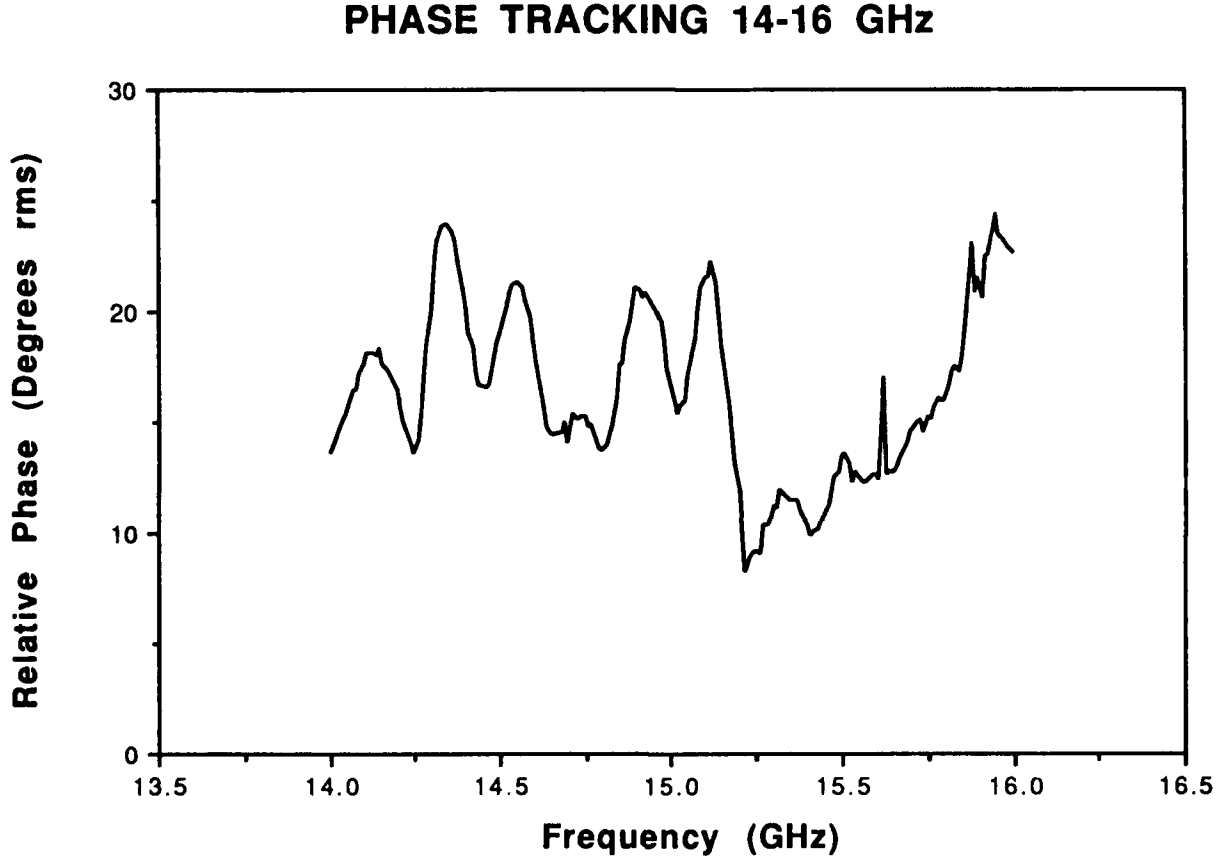
START 16.000000000 GHz
STOP 18.000000000 GHz

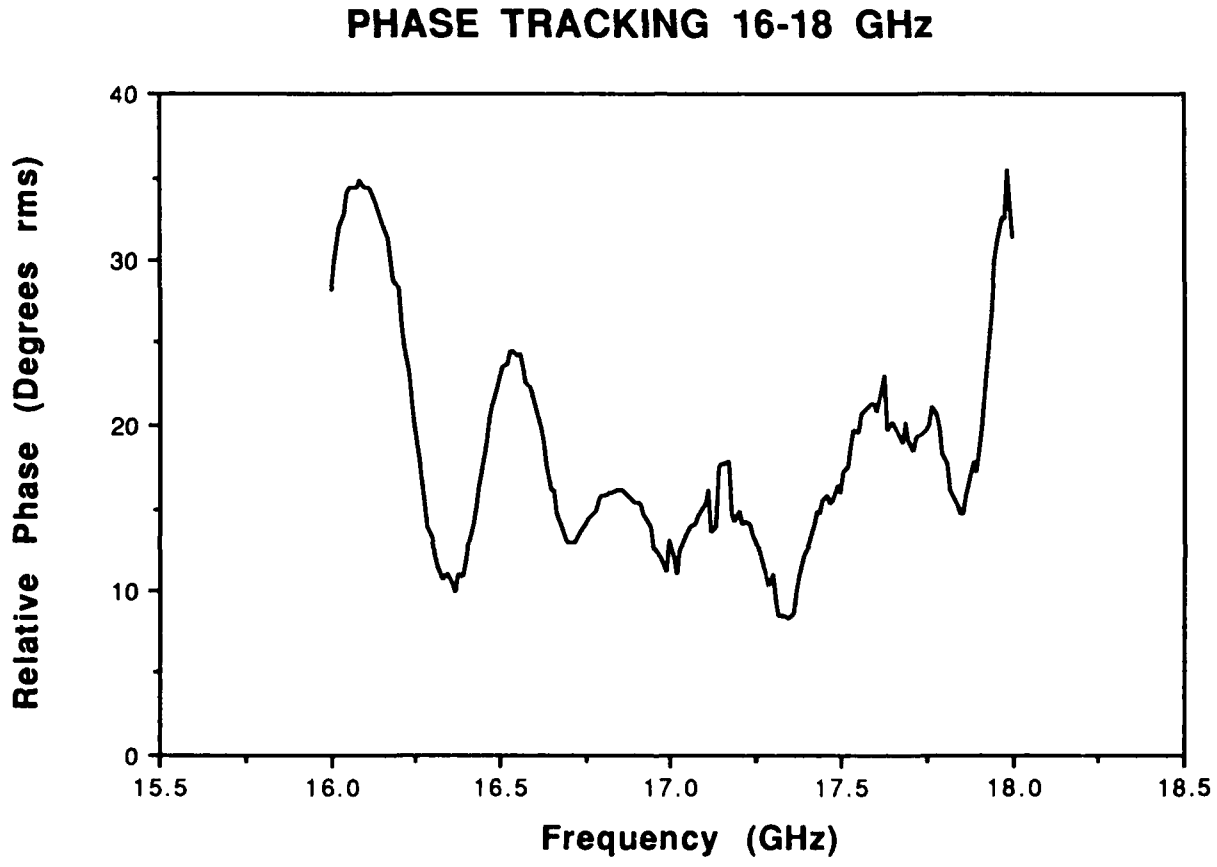

PHASE TRACKING 6-8 GHz
Relative Phase (Degrees rms)
30
20
10
0
5.5
6.0
6.5
7.0
7.5
8.0
8.5
Frequency (GHz)

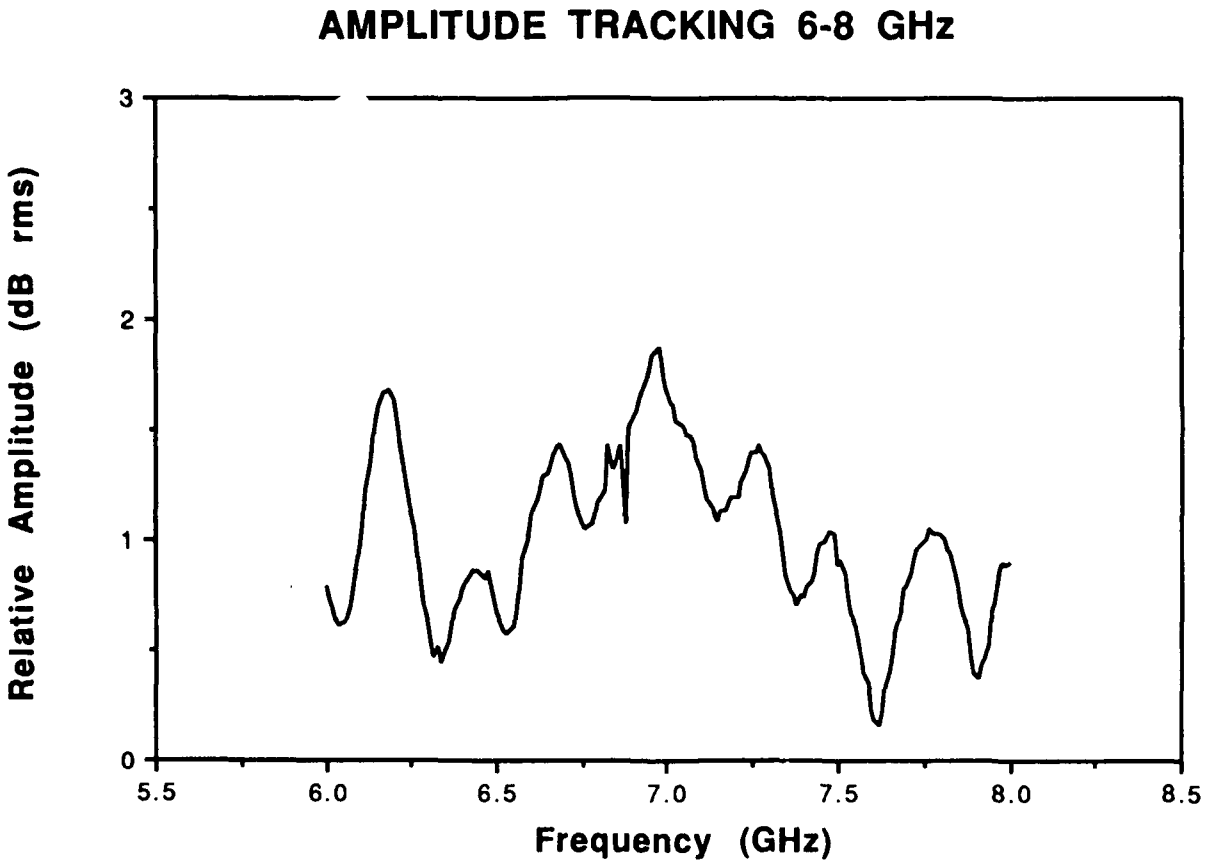

PHASE TRACKING 8-10 GHz
Relative Phase (Degrees rms)
20
10
0
7.5
8.0
8.5
9.0
9.5
10.0
10.5
Frequency (GHz)

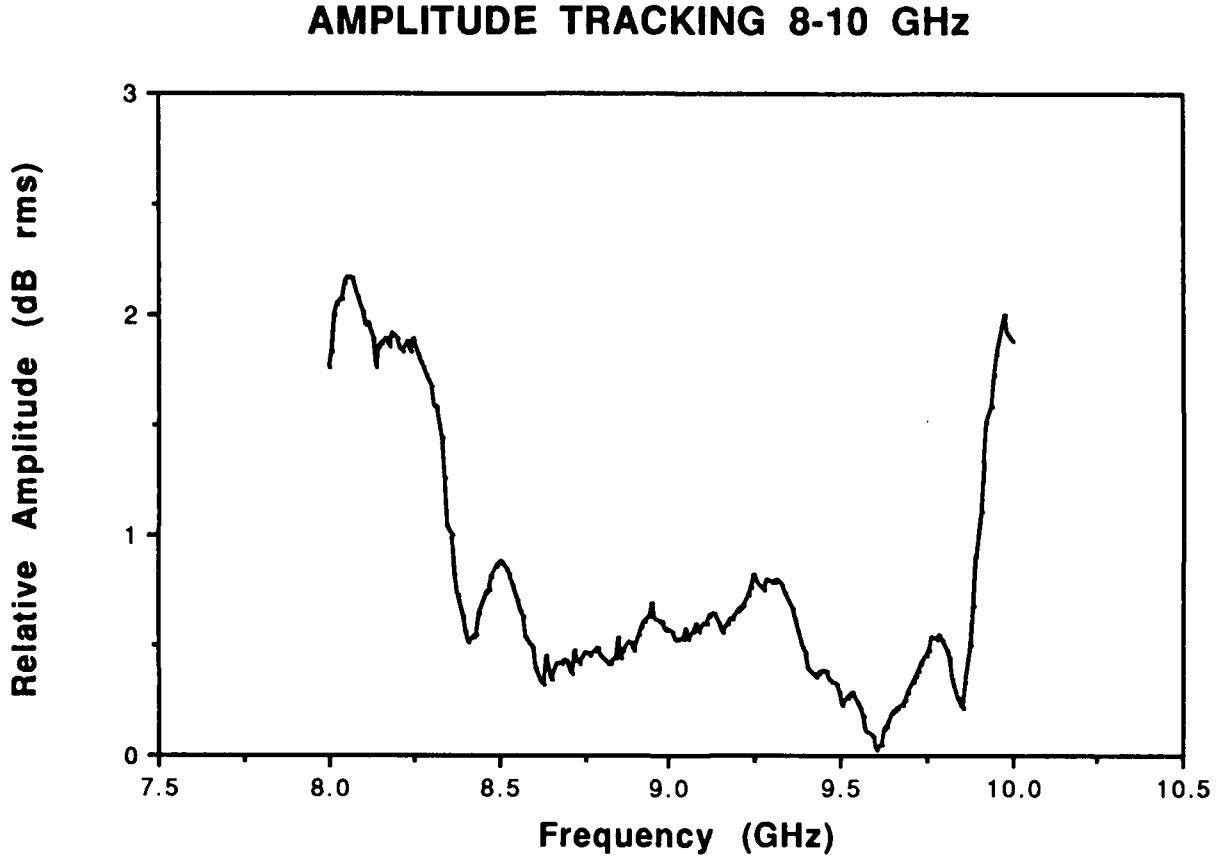

PHASE TRACKING 10-12 GHz
Relative Phase (Degrees rms)
40
30
20
10
0
9.5
10.0
10.5
11.0
11.5
12.0
12.5
Frequency (GHz)


PHASE TRACKING 12-14 GHz
Relative Phase (Degrees rms)
40
30
20
10
0
11.5
12.0
12.5
13.0
13.5
14.0
14.5
Frequency (GHz)

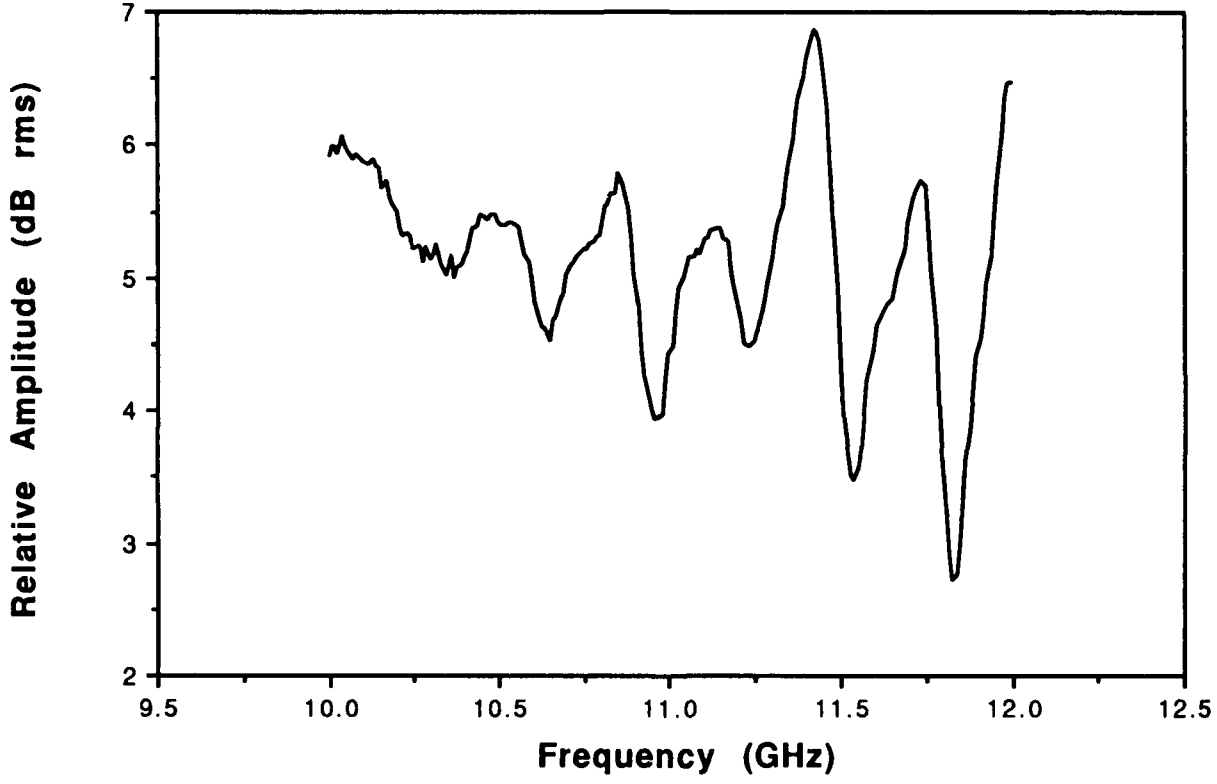

PHASE TRACKING 14-16 GHz
Relative Phase (Degrees rms)
30
20
10
0
13.5
14.0
14.5
15.0
15.5
16.0
16.5
Frequency (GHz)

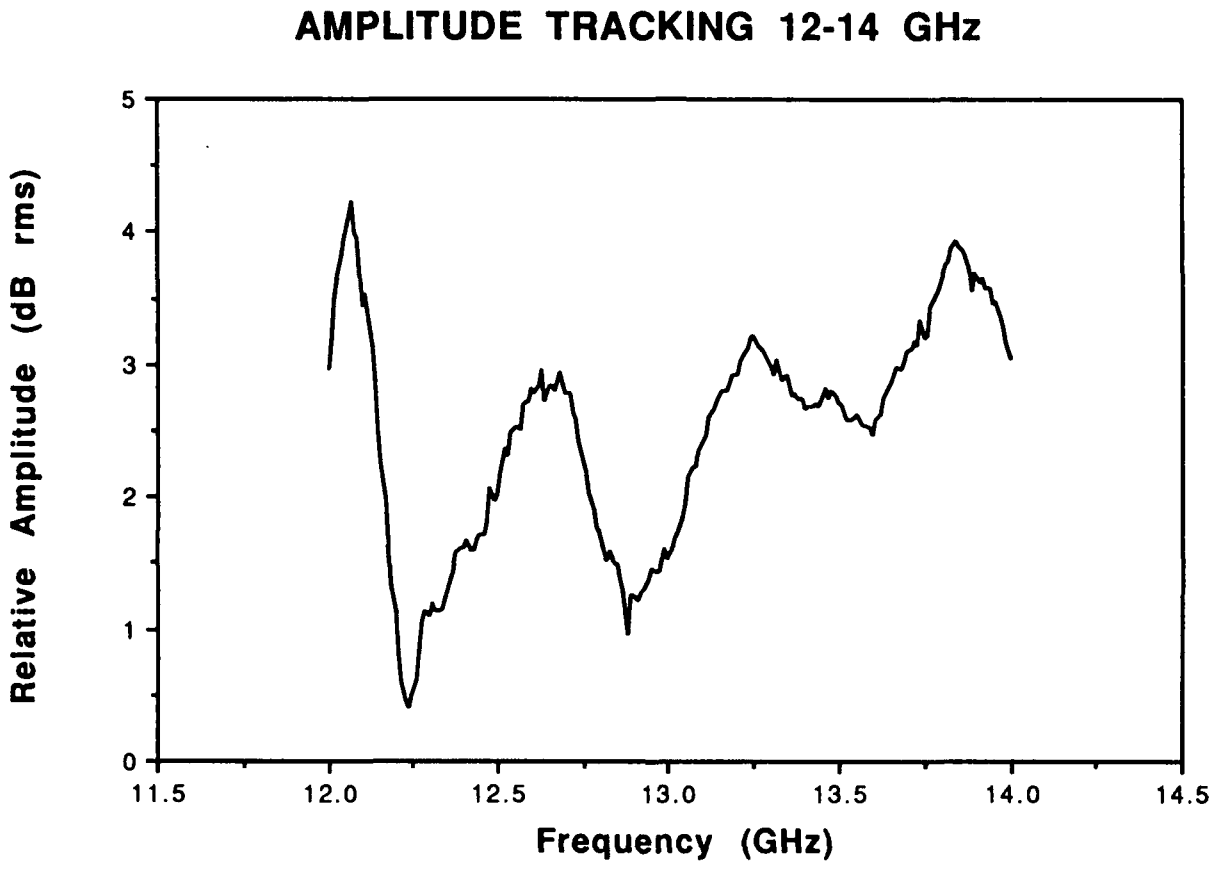

PHASE TRACKING 16-18 GHz
Relative Phase (Degrees rms)
40
30
20
10
0
15.5
16.0
16.5
17.0
17.5
18.0
18.5
Frequency (GHz)

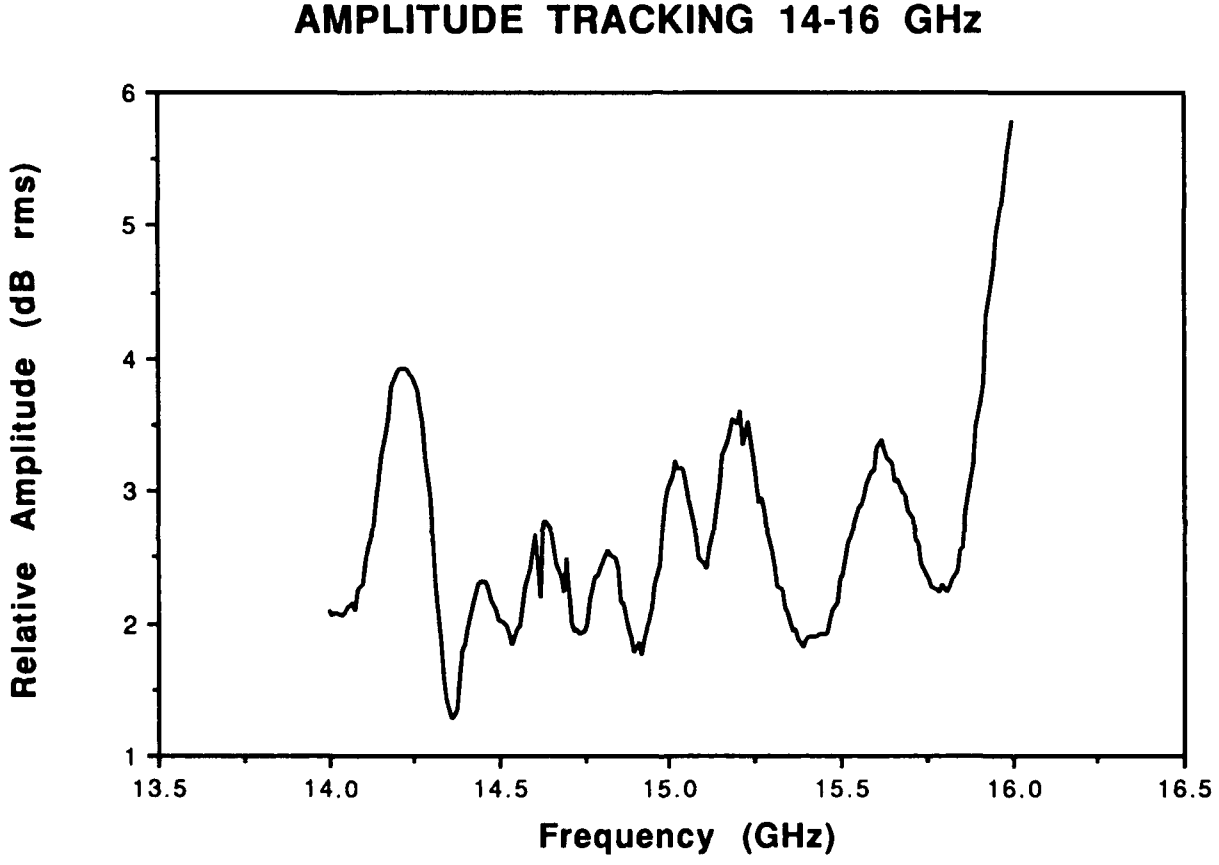

AMPLITUDE TRACKING 6-8 GHz
Relative Amplitude (dB rms)
3
2
1
0
5.5
6.0
6.5
7.0
7.5
8.0
8.5
Frequency (GHz)


AMPLITUDE TRACKING 8-10 GHz
Relative Amplitude (dB rms)
3
2
1
0
7.5
8.0
8.5
9.0
9.5
10.0
10.5
Frequency (GHz)

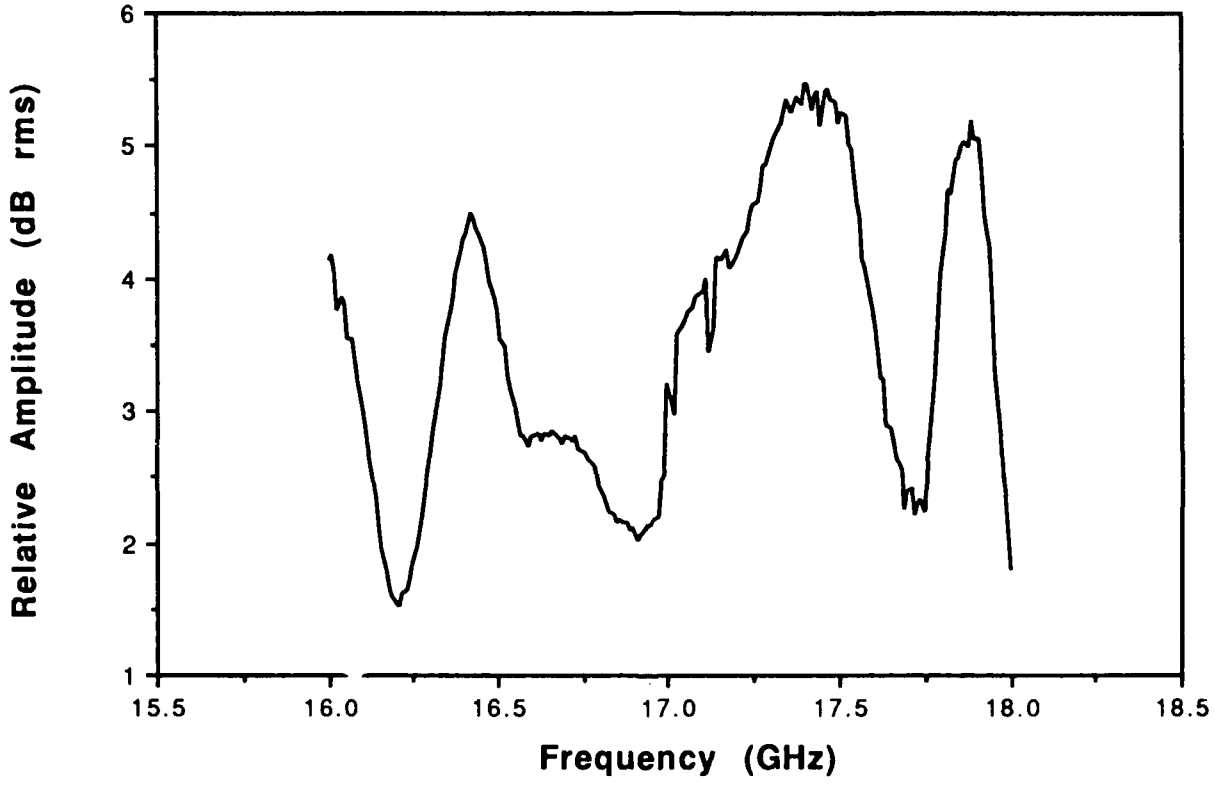
AMPLITUDE TRACKING 10-12 GHz




AMPLITUDE TRACKING 12-14 GHz
Relative Amplitude (dB rms)
5
4
3
2
1
0
11.5
12.0
12.5
13.0
13.5
14.0
14.5
Frequency (GHz)


AMPLITUDE TRACKING 14-16 GHz
Relative Amplitude (dB rms)
6
5
4
3
2
1
13.5
14.0
14.5
15.0
15.5
16.0
16.5
Frequency (GHz)

AMPLITUDE TRACKING 16-18 GHz



Appendix C

Drawings, Wire Lists, etc.

Appendix C

Drawings, Wire Lists, etc.

This Appendix contains connector pin-outs, wire lists, schematics, etc.

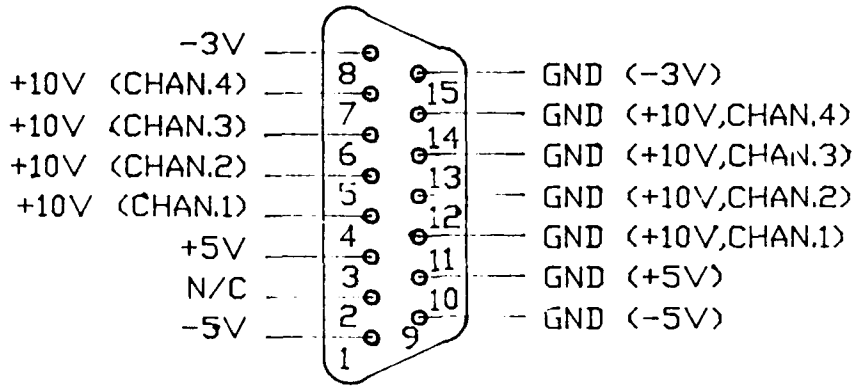


Figure C-1. Input power connector - J1.

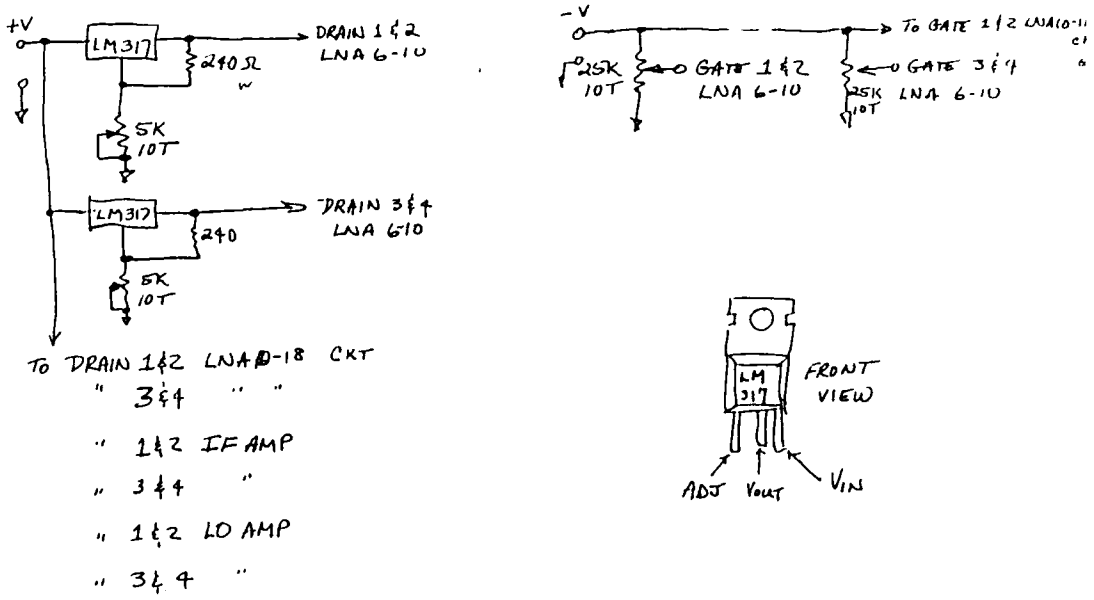


Figure C-2. Voltage regulator schematic.

INPUT POWER CONNECTOR TO CHANNEL 1

PG 1 of 1

WIRE NUMBER	WIRE SIZE	WIRE COLOR	WIRE LENGTH	CIRCUIT FROM	CIRCUIT TO	FUNCTION
				J1-1	P7-2	SWITCH DRIVER -5 VOLTS
				J1-2	N/C	
				J1-3	P7-4	SWITCH DRIVER +5 VOLTS
				J1-4	P7-6	+10 VOLTS
				J1-5	N/C	
				J1-6	N/C	
				J1-7	N/C	
				J1-8	P7-8	-3 VOLTS TO GATES
				J1-9	P7-1	-5 VOLT GND
				J1-10	P7-3	+5 VOLT GND
				J1-11	P7-5	CHANNEL 1 +10 VOLT GND
				J1-12	N/C	
				J1-13	N/C	
				J1-14	N/C	
				J1-15	P7-7	-3 VOLT GND

INPUT POWER CONNECTOR TO CHANNEL 2 | PG 1 of 1

WIRE NUMBER	WIRE SIZE AWG	WIRE COLOR	WIRE LENGTH	CIRCUIT FROM	CIRCUIT TO	FUNCTION
				J1-1	P6-2	SWITCH DRIVER -5 VOLTS
				J1-2	N/C	
				J1-3	P6-4	SWITCH DRIVER +5 VOLTS
				J1-4	N/C	
				J1-5	P6-6	+10 VOLTS
				J1-6	N/C	
				J1-7	N/C	
				J1-8	P6-8	-3 VOLTS TO GATES
				J1-9	P6-1	-5 VOLT GND
				J1-10	P6-3	+5 VOLT GND
				J1-11	N/C	
				J1-12	P6-5	CHANNEL 2 +10 VOLT GND
				J1-13	N/C	
				J1-14	N/C	
				J1-15	P6-7	-3 VOLT GND

INPUT POWER CONNECTOR TO CHANNEL 3 | PG 1 of 1

WIRE NUMBER	WIRE SIZE Awg	WIRE COLOR	WIRE LENGTH	CIRCUIT FROM	CIRCUIT TO	FUNCTION
				J1-1	P5-2	SWITCH DRIVER -5 VOLTS
				J1-2	N/C	
				J1-3	P5-4	SWITCH DRIVER +5 VOLTS
				J1-4	N/C	
				J1-5	N/C	
				J1-6	P5-6	+10 VOLTS
				J1-7	N/C	
				J1-8	P5-8	-3 VOLTS TO GATES
				J1-9	P5-1	-5 VOLT GND
				J1-10	P5-3	+5 VOLT GND
				J1-11	N/C	
				J1-12	N/C	
				J1-13	P5-5	CHANNEL 3 +10 VOLT GND
				J1-14	N/C	
				J1-15	P5-7	-3 VOLT GND

INPUT POWER CONNECTOR TO CHANNEL 4 | PG 1 of 1

WIRE NUMBER	WIRE SIZE		WIRE COLOR	WIRE LENGTH	CIRCUIT			FUNCTION
		Awg			FROM	TO		
					J1-1	P4-2		SWITCH DRIVER -5 VOLTS
					J1-2	N/C		
					J1-3	P4-4		SWITCH DRIVER +5 VOLTS
					J1-4	N/C		
					J1-5	N/C		
					J1-6	N/C		
					J1-7	P4-6		+10 VOLTS
					J1-8	P4-8		-3 VOLTS TO GATES
					J1-9	P4-1		-5 VOLT GND
					J1-10	P4-3		+5 VOLT GND
					J1-11	N/C		
					J1-12	N/C		
					J1-13	N/C		
					J1-14	P4-5		CHANNEL 4 +10 VOLT GND
					J1-15	P4-7		-3 VOLT GND

SWITCH CONTROL

SUBBAND SWITCH POSITION	FREQUENCY RANGE	REQUIRED L.O. FREQUENCY	CONNECTOR PIN J2-14	J2-15	J2-16	J2-17	J2-18	J2-19
1	6-8 GHz	11 GHz	0	1	1	1	1	1
2	8-10 GHz	13 GHz	1	0	1	1	1	1
3	10-12 GHz	15 GHz	1	1	0	1	1	1
4	12-14 GHz	17 GHz	1	1	1	0	1	1
5	14-16 GHz	11 GHz	1	1	1	1	0	1
6	16-18 GHz	13 GHz	1	1	1	1	1	0

0 = ON (GROUNDED)
1= OFF (OPEN)

REV. A- CHANGED SUB-BAND SEQUENCE ON CONN. PINS

PIN 19 WAS 6-8 GHz
PIN 18 WAS 8-10 GHz
PIN 17 WAS 10-12 GHz
PIN 16 WAS 12-14 GHz
PIN 15 WAS 14-16 GHz
PIN 14 WAS 16-18 GHz

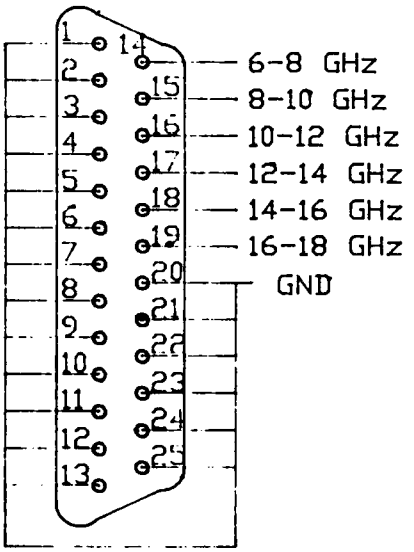


Figure C-3. Switch control box.

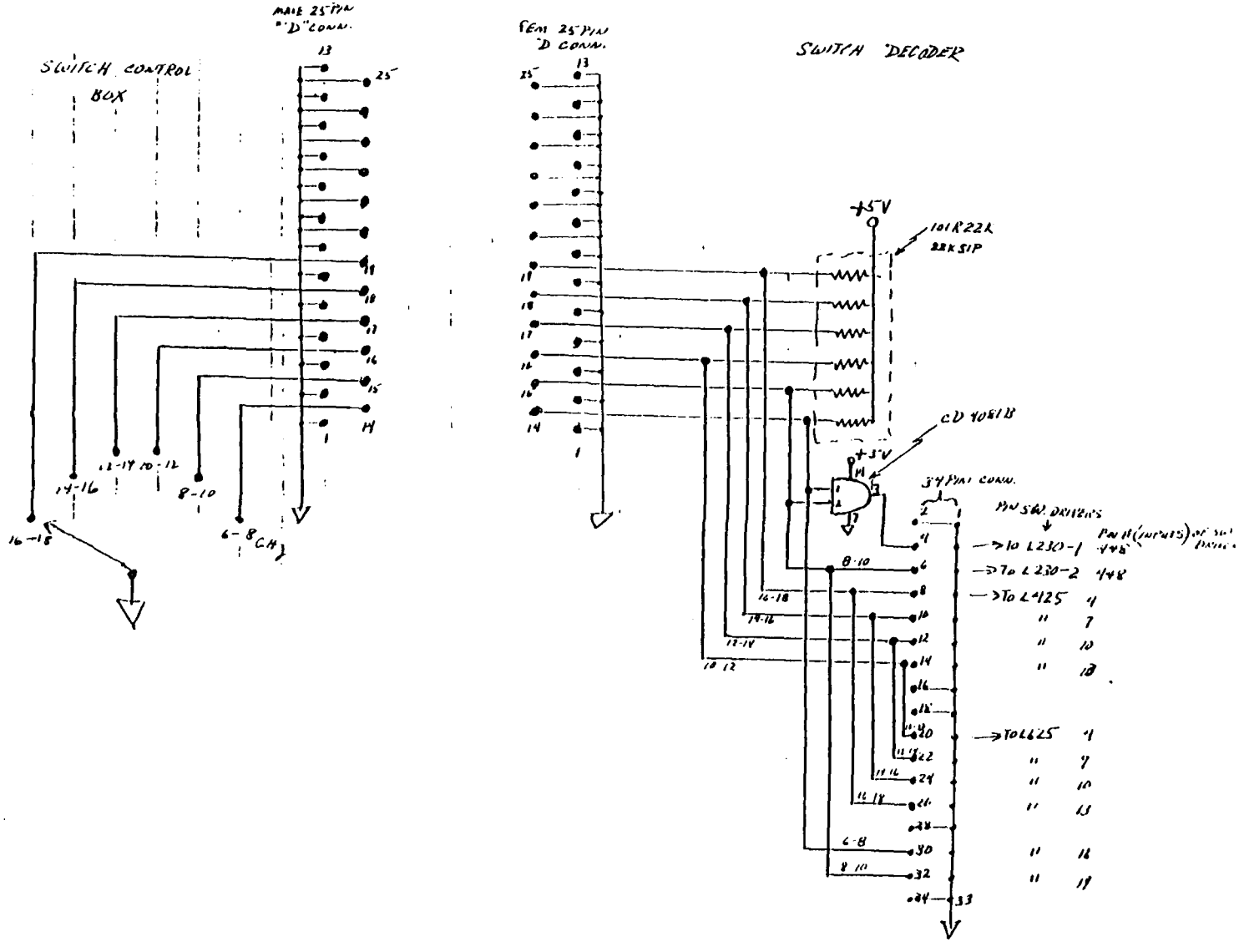


Figure C-4. Switch control schematic.

SWITCH DRIVER DECODER TO SWITCH DRIVERS

WIRE NUMBER	WIRE SIZE	WIRE COLOR	WIRE LENGTH	CIRCUIT FROM	CIRCUIT TO	FUNCTION	
	Awg.						
				J3-4	L230-1	2T SW DRIVER	ALL FOUR CHANNELS
				J3-6	L230-2	2T SW DRIVER	
				J3-8	L425-4	4T SW DRIVER	ALL FOUR CHANNELS
				J3-10	L425-7	4T SW DRIVER	
				J3-12	L425-10	4T SW DRIVER	
				J3-14	L425-13	4T SW DRIVER	
				J3-20	L625-4	6T SW DRIVER	ALL FOUR CHANNELS
				J3-22	L625-7	6T SW DRIVER	
				J3-24	L625-10	6T SW DRIVER	
				J3-26	L625-13	6T SW DRIVER	
				J3-30	L625-16	6T SW DRIVER	
				J3-32	L625-19	6T SW DRIVER	
				J3-1	DC GND	GND UNUSED PIN	
				J3-2	DC GND	GND UNUSED PIN	
				J3-3	DC GND	GND UNUSED PIN	
				J3-5	DC GND	GND UNUSED PIN	
				J3-7	DC GND	GND UNUSED PIN	
				J3-9	DC GND	GND UNUSED PIN	
				J3-11	DC GND	GND UNUSED PIN	
				J3-15	DC GND	GND UNUSED PIN	
				J3-17	DC GND	GND UNUSED PIN	
				J3-18	DC GND	GND UNUSED PIN	

SWITCH DRIVER DECODER TO SWITCH DRIVERS

WIRE NUMBER	WIRE SIZE		WIRE COLOR	WIRE LENGTH	CIRCUIT			FUNCTION
		Awg			FROM	TO		
					J3-19	DC GND		GND UNUSED PIN
					J3-21	DC GND		GND UNUSED PIN
					J3-23	DC GND		GND UNUSED PIN
					J3-25	DC GND		GND UNUSED PIN
					J3-27	DC GND		GND UNUSED PIN
					J3-29	DC GND		GND UNUSED PIN
					J3-31	DC GND		GND UNUSED PIN
					J3-33	DC GND		GND UNUSED PIN
					J3-34	DC GND		GND UNUSED PIN

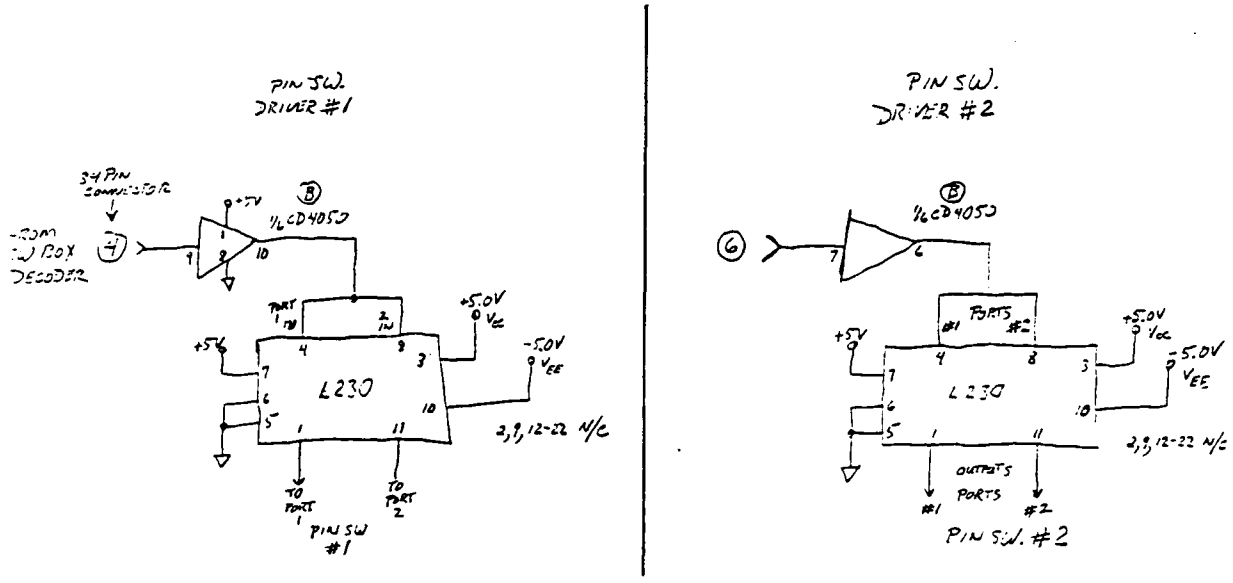


Figure C-5. Two-throw switch, driver schematic.

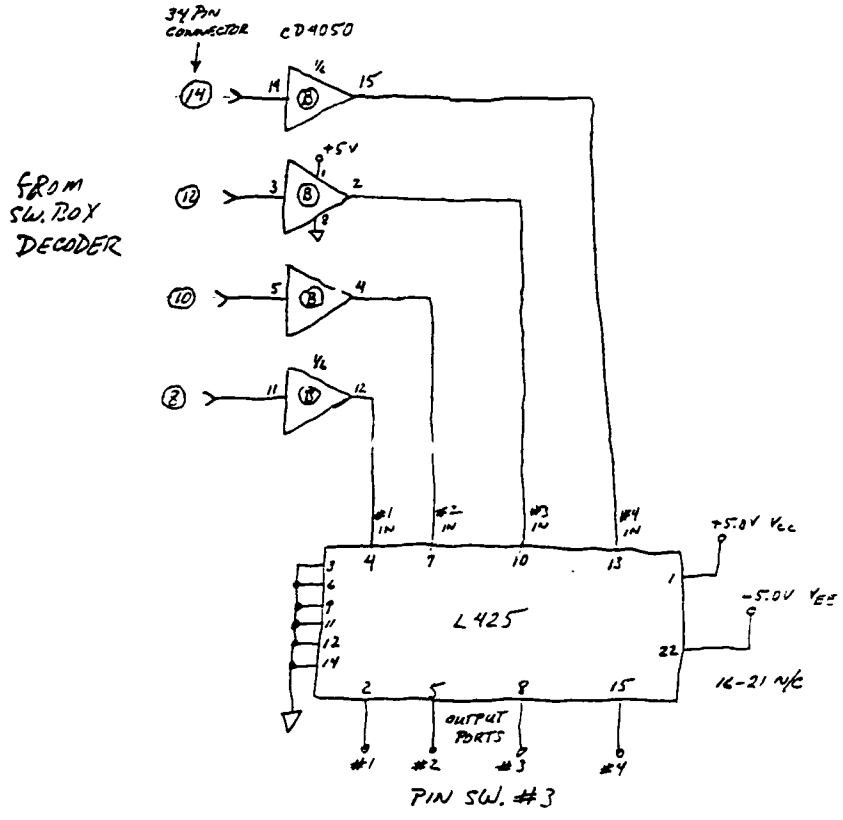


Figure C-6. Four-throw switch, driver schematic.

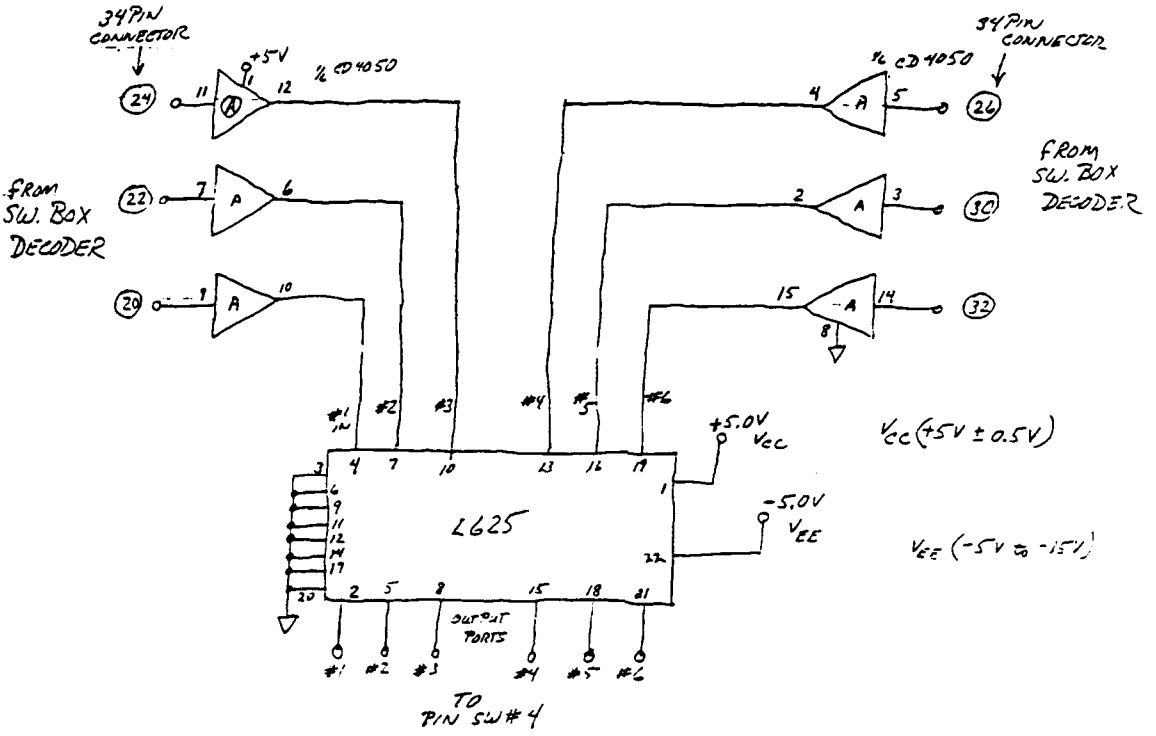


Figure C-7. Six-throw switch, driver schematic.

CONTROL BOX CONNECTOR TO SWITCH DRIVER DECODER

PG 1 of 1

WIRE NUMBER	WIRE SIZE Awg	WIRE COLOR	WIRE LENGTH	CIRCUIT FROM	CIRCUIT TO	FUNCTION
				J2-14	P3-30	SUB-BAND 6-8 GHz
				J2-15	P3-6	SUB-BAND 8-10 GHz
				J2-16	P3-14	SUB-BAND 10-12 GHz
				J2-17	P3-12	SUB-BAND 12-14 GHz
				J2-18	P3-10	SUB-BAND 14-16 GHz
				J2-19	P3-8	SUB-BAND 16-18 GHz
				J2-1 THRU 13	GND	DC GND
				J2-20 THRU 25	GND	DC GND